FIG. 1

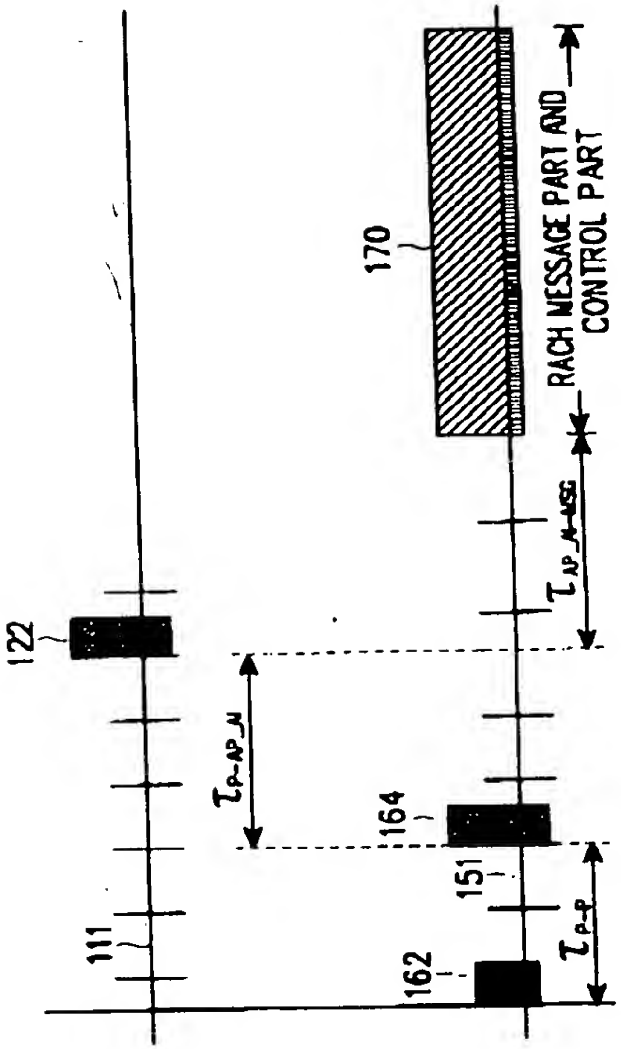


FIG. 2

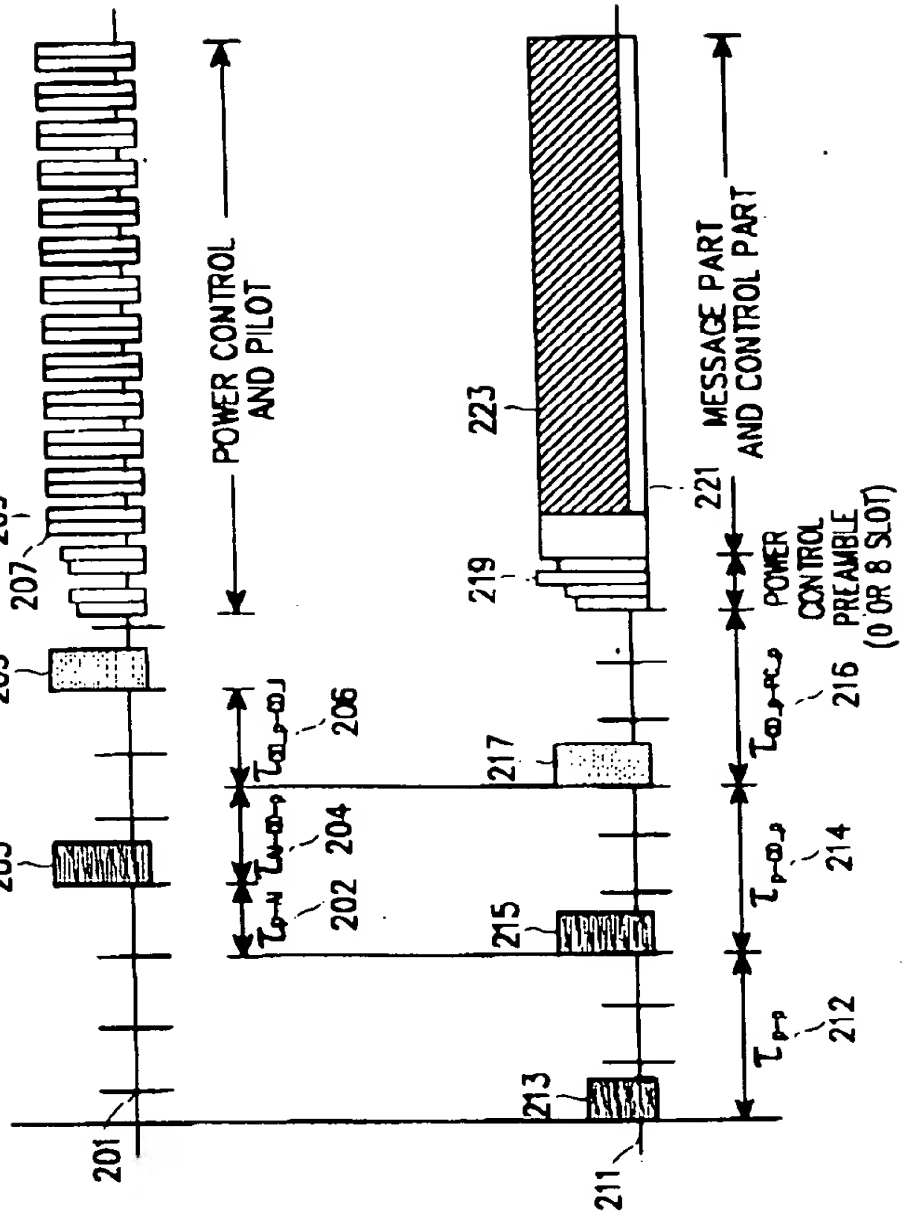
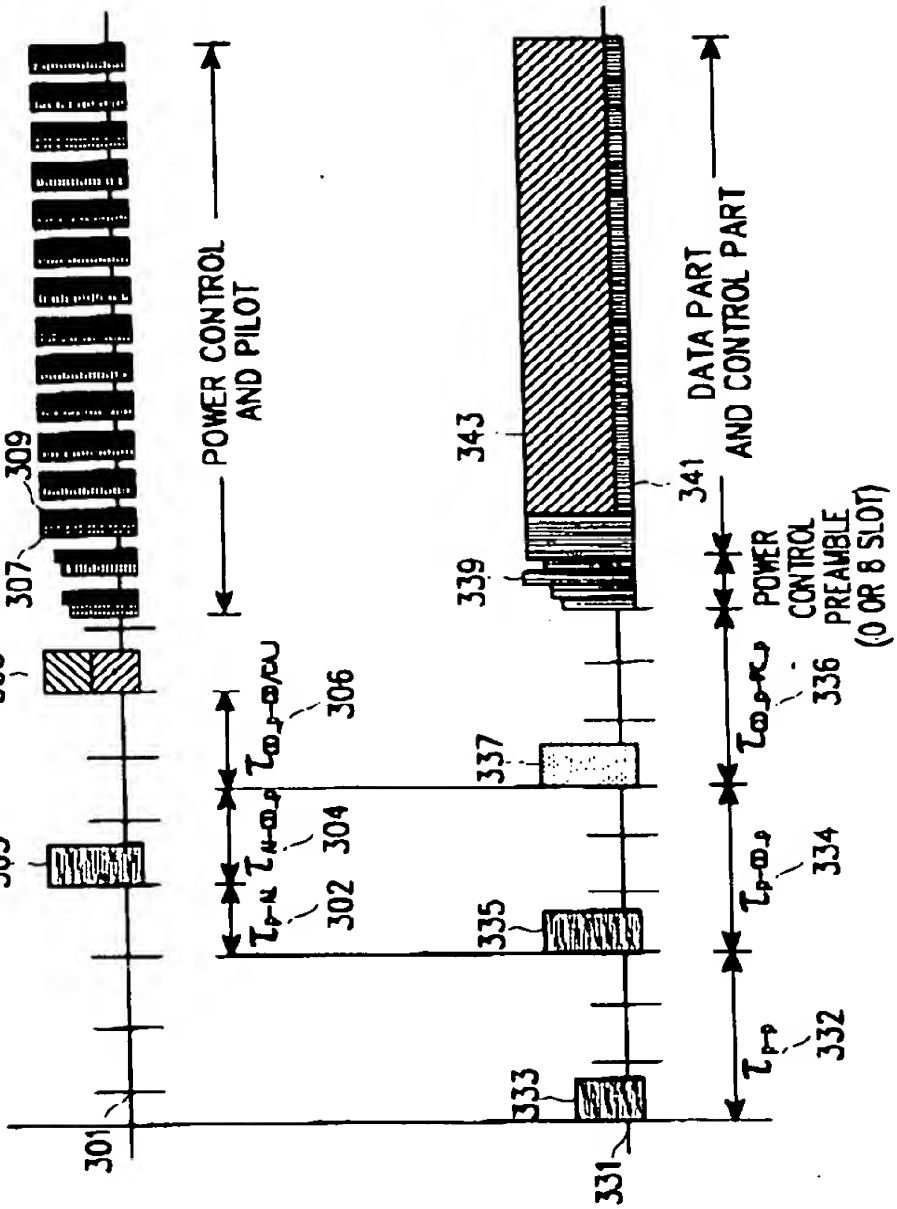

POWER CONTROL AND PILOT
MESSAGE PART AND CONTROL PART
POWER CONTROL PREAMBLE (0 OR 8 SLOT)
201
202
203
204
205
206
207
209
211
212
213
214
215
216
217
219
221
223

FIG. 3


POWER CONTROL AND PILOT
DATA PART AND CONTROL PART
POWER CONTROL PREAMBLE (0 OR 8 SLOT)
301
302
303
304
305
306
307
309
331
332
333
334
335
336
337
339
341
343

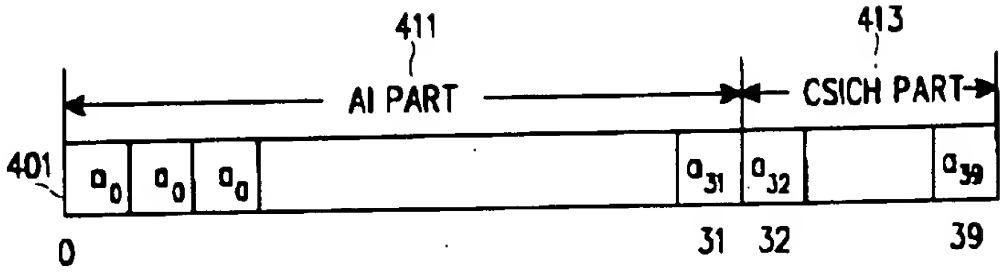

411
413
AI PART
CSICH PART
401
a_0
a_0
a_0
a_{31}
a_{32}
a_{39}
0
31
32
39

FIG. 4A

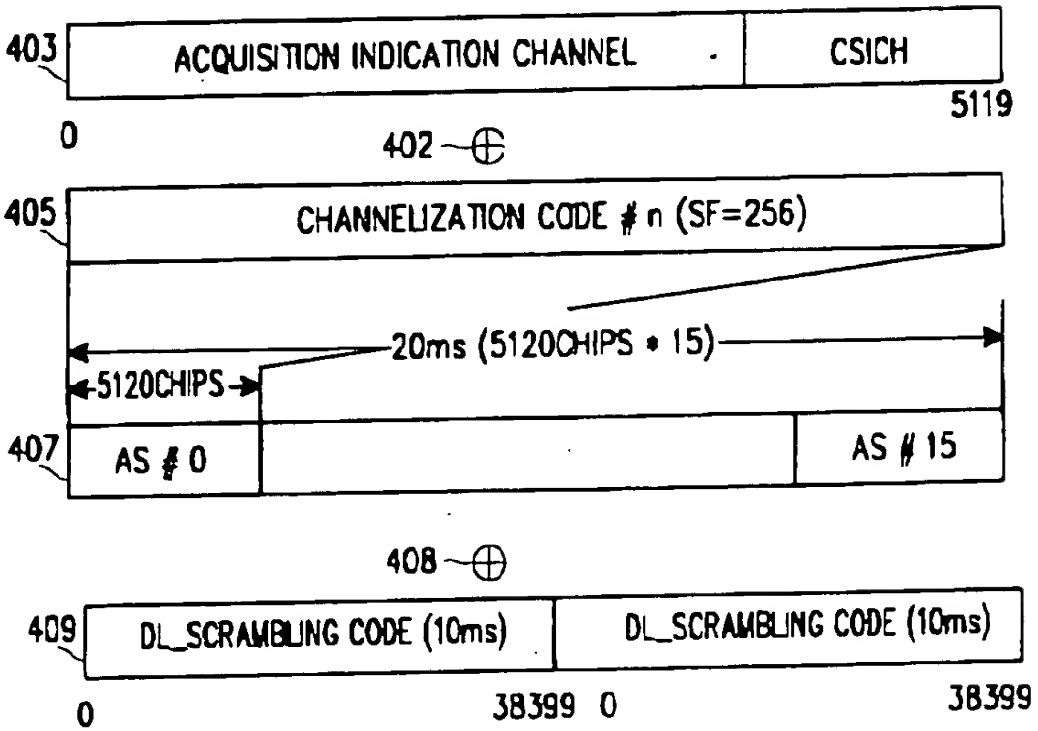

403
ACQUISITION INDICATION CHANNEL
CSICH
0
5119
402
405
CHANNELIZATION CODE # n (SF=256)
20ms (5120CHIPS * 15)
5120CHIPS
407
AS # 0
AS # 15
408
409
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399

FIG. 4B

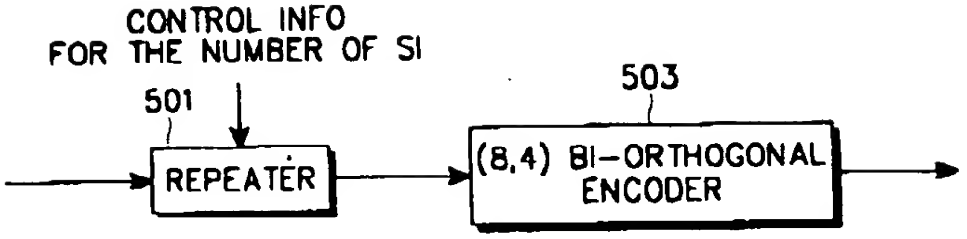

CONTROL INFO
FOR THE NUMBER OF SI
501
503
REPEATER
(8,4) BI-ORTHOGONAL
ENCODER

FIG. 5

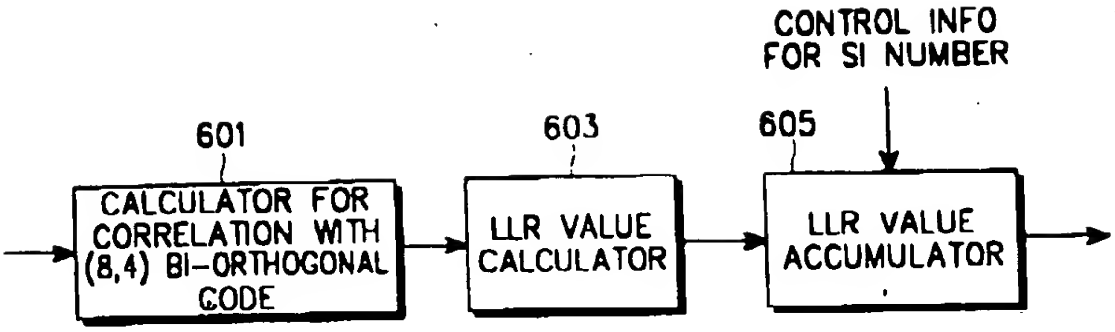
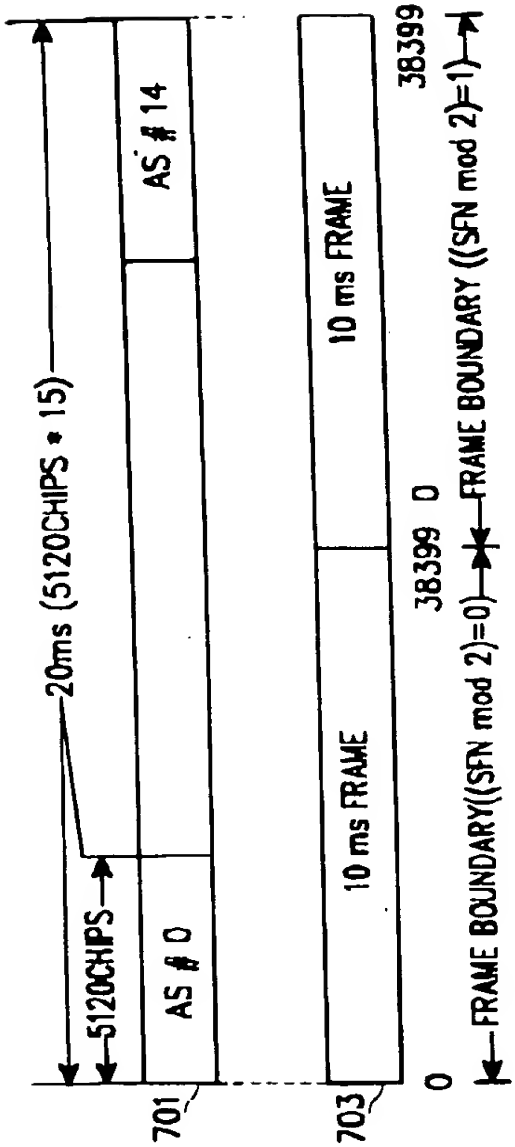

CONTROL INFO
FOR SI NUMBER
601
603
605
CALCULATOR FOR CORRELATION WITH (8,4) BI-ORTHOGONAL CODE
LLR VALUE CALCULATOR
LLR VALUE ACCUMULATOR

FIG. 6

FIG. 7


20ms (5120CHIPS * 15)
5120CHIPS
AS # 0
AS # 14
10 ms FRAME
10 ms FRAME
701
703
0
38399
38399 0
FRAME BOUNDARY((SFN mod 2)=0)
FRAME BOUNDARY ((SFN mod 2)=1)

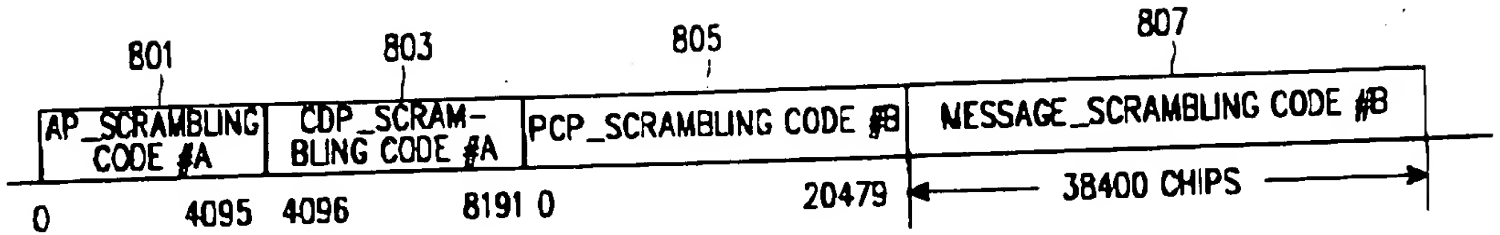

801
803
805
807
AP_SCRAMBLING CODE #A
CDP_SCRAM-BLING CODE #A
PCP_SCRAMBLING CODE #B
MESSAGE_SCRAMBLING CODE #B
0
4095
4096
8191
0
20479
38400 CHIPS

FIG. 8A

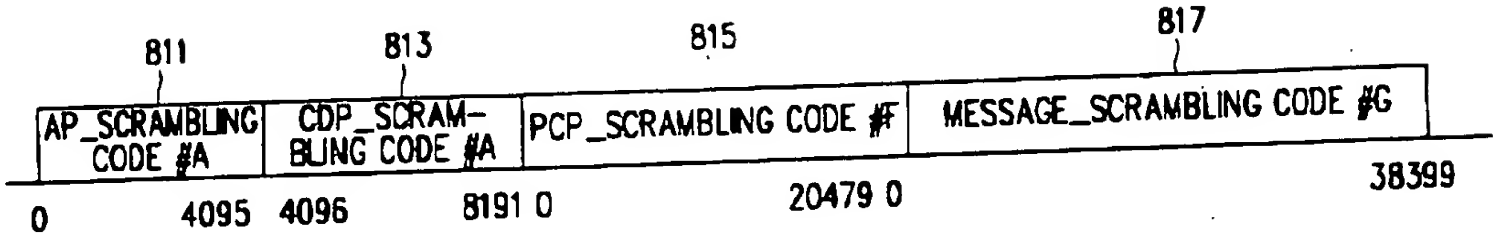

811
813
815
817
AP_SCRAMBLING CODE #A
CDP_SCRAM-BLING CODE #A
PCP_SCRAMBLING CODE #F
MESSAGE_SCRAMBLING CODE #G
0
4095
4096
8191
0
20479
0
38399

FIG. 8B

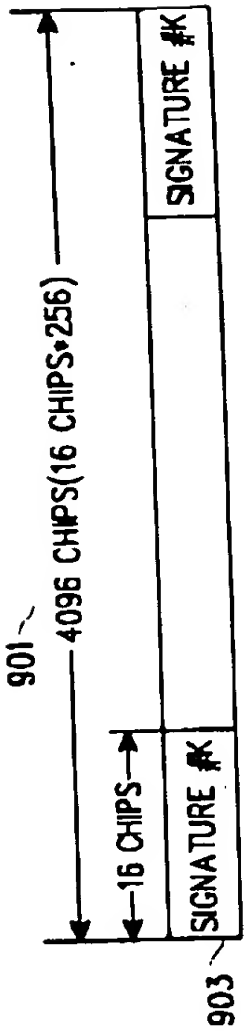

901
4096 CHIPS(16 CHIPS*256)
16 CHIPS
SIGNATURE #K
SIGNATURE #K
903

FIG. 9A

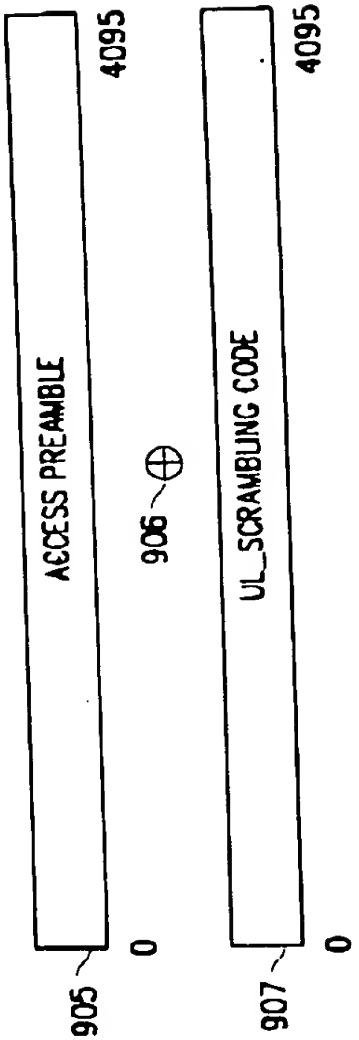

ACCESS PREAMBLE
4095
0
905
906
UL_SCRAMBLING CODE
4095
0
907

FIG. 9B

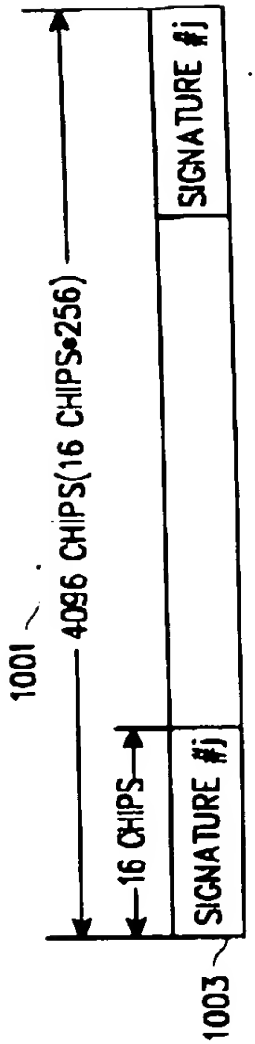


FIG. 10A

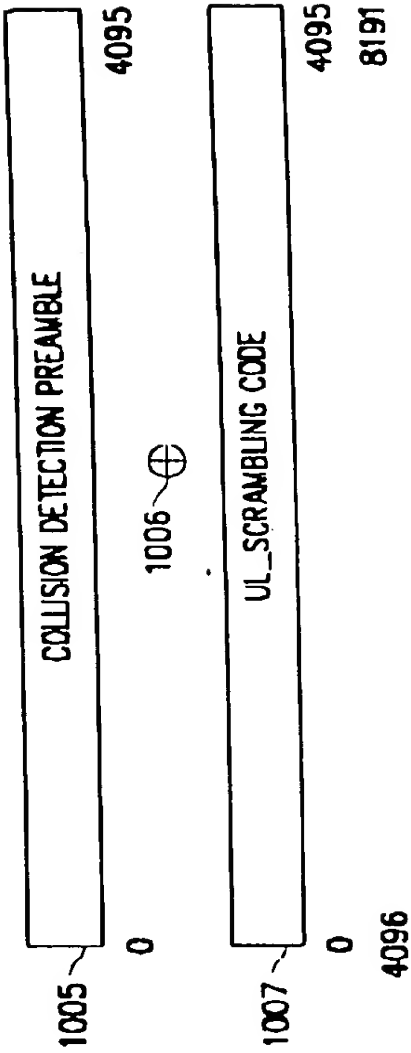


FIG. 10B

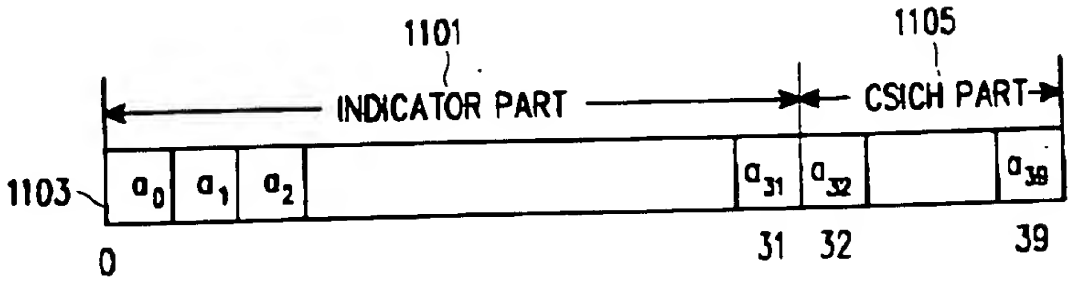


FIG. 11A

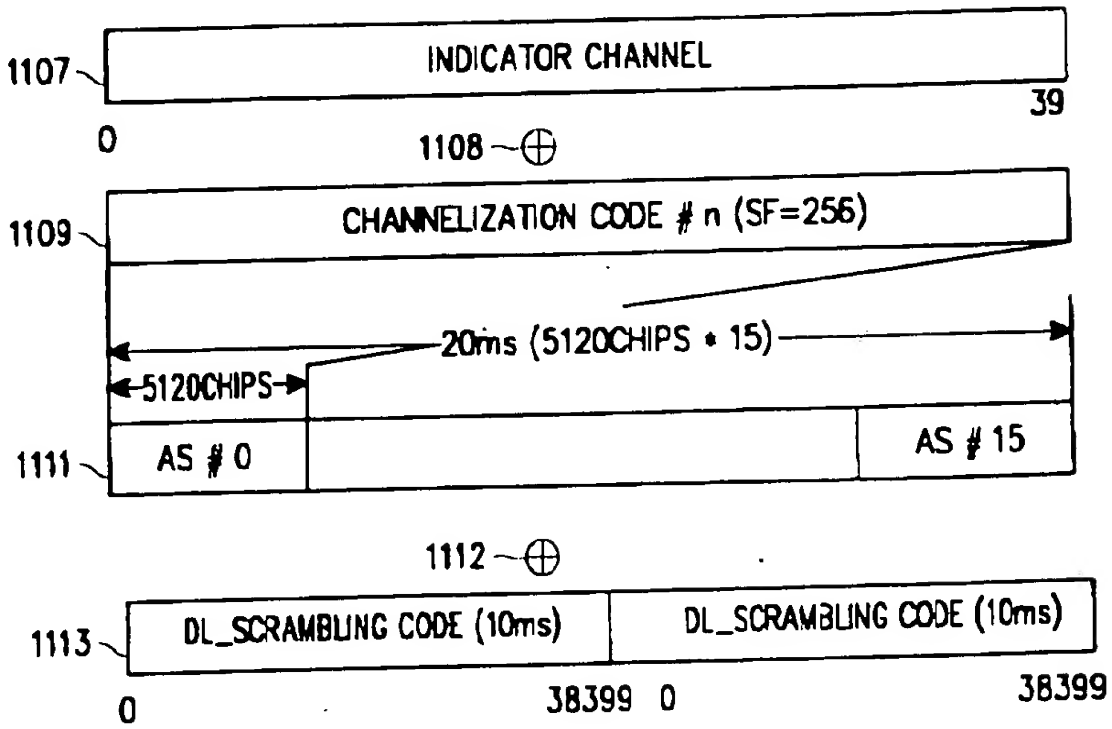


FIG. 11B

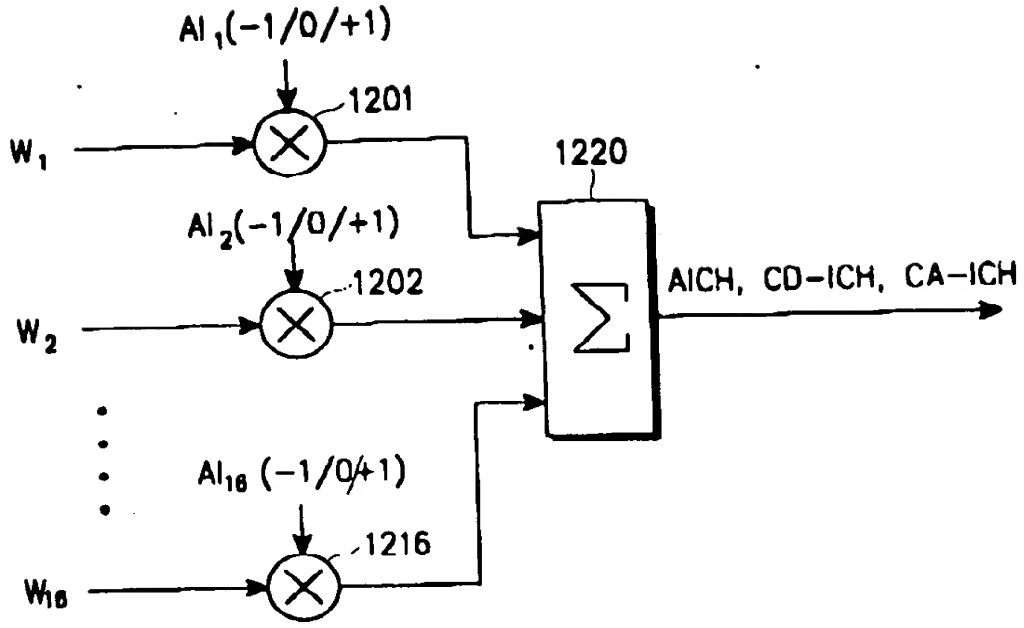

AI1(-1/0/+1)
1201
W1
1220
AI2(-1/0/+1)
1202
W2
AICH, CD-ICH, CA-ICH
AI16 (-1/0/+1)
1216
W16

FIG. 12

FIG. 13A

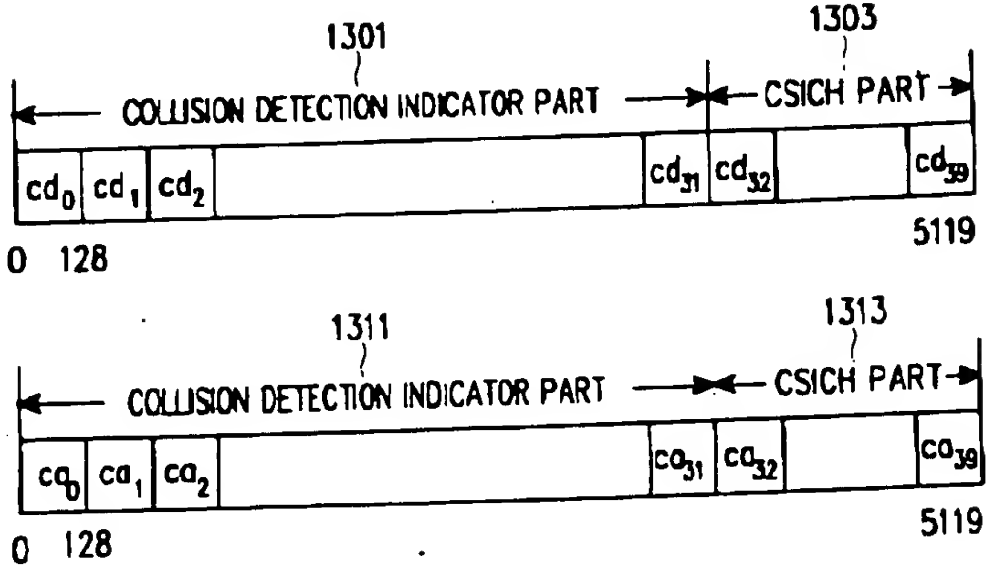
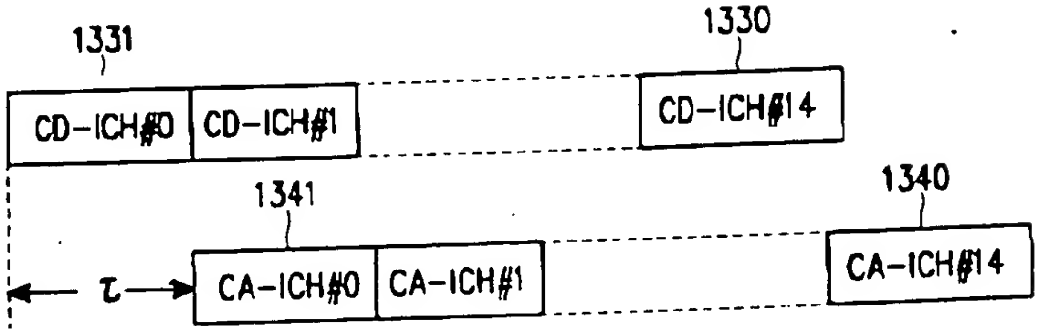


FIG. 13B



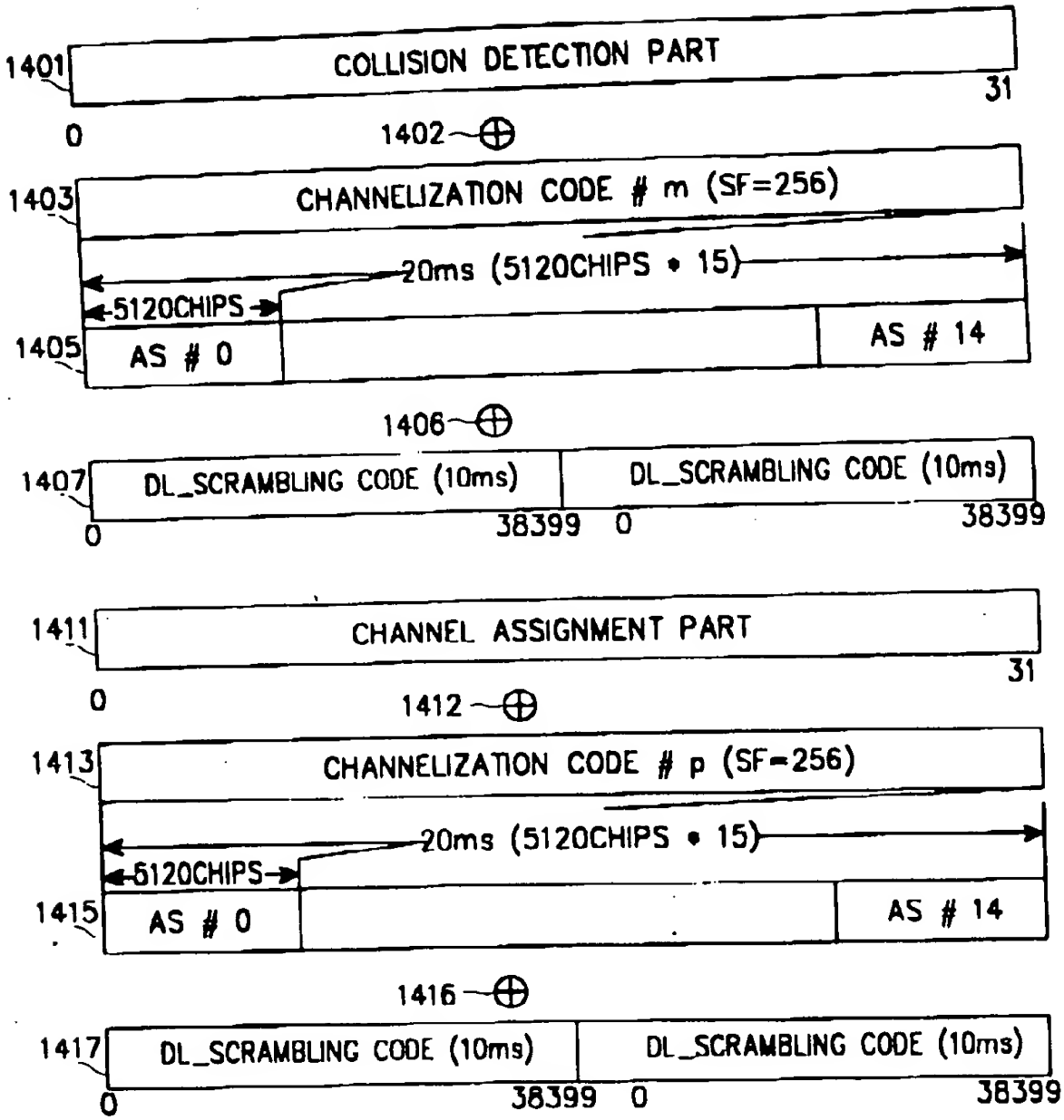

1401
COLLISION DETECTION PART
31
0
1402
1403
CHANNELIZATION CODE # m (SF=256)
20ms (5120CHIPS • 15)
5120CHIPS
1405
AS # 0
AS # 14
1406
1407
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399
1411
CHANNEL ASSIGNMENT PART
31
0
1412
1413
CHANNELIZATION CODE # p (SF=256)
20ms (5120CHIPS • 15)
5120CHIPS
1415
AS # 0
AS # 14
1416
1417
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399

FIG. 14

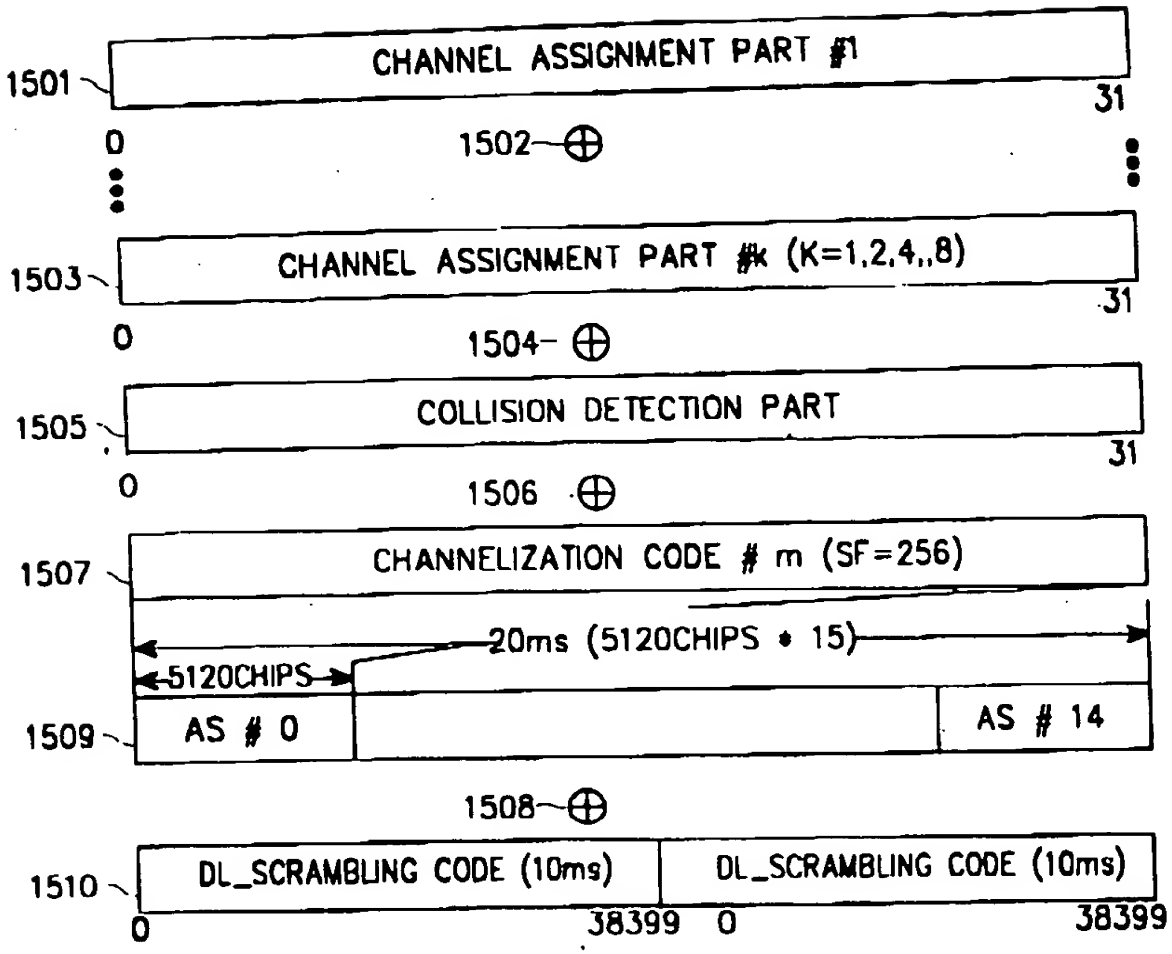

1501
CHANNEL ASSIGNMENT PART #1
0
31
1502
1503
CHANNEL ASSIGNMENT PART #k (K=1,2,4,,8)
0
31
1504
1505
COLLISION DETECTION PART
0
31
1506
1507
CHANNELIZATION CODE # m (SF=256)
20ms (5120CHIPS * 15)
5120CHIPS
1509
AS # 0
AS # 14
1508
1510
DL_SCRAMBLING CODE (10ms)
DL_SCRAMBLING CODE (10ms)
0
38399
0
38399

FIG. 15

FIG. 16

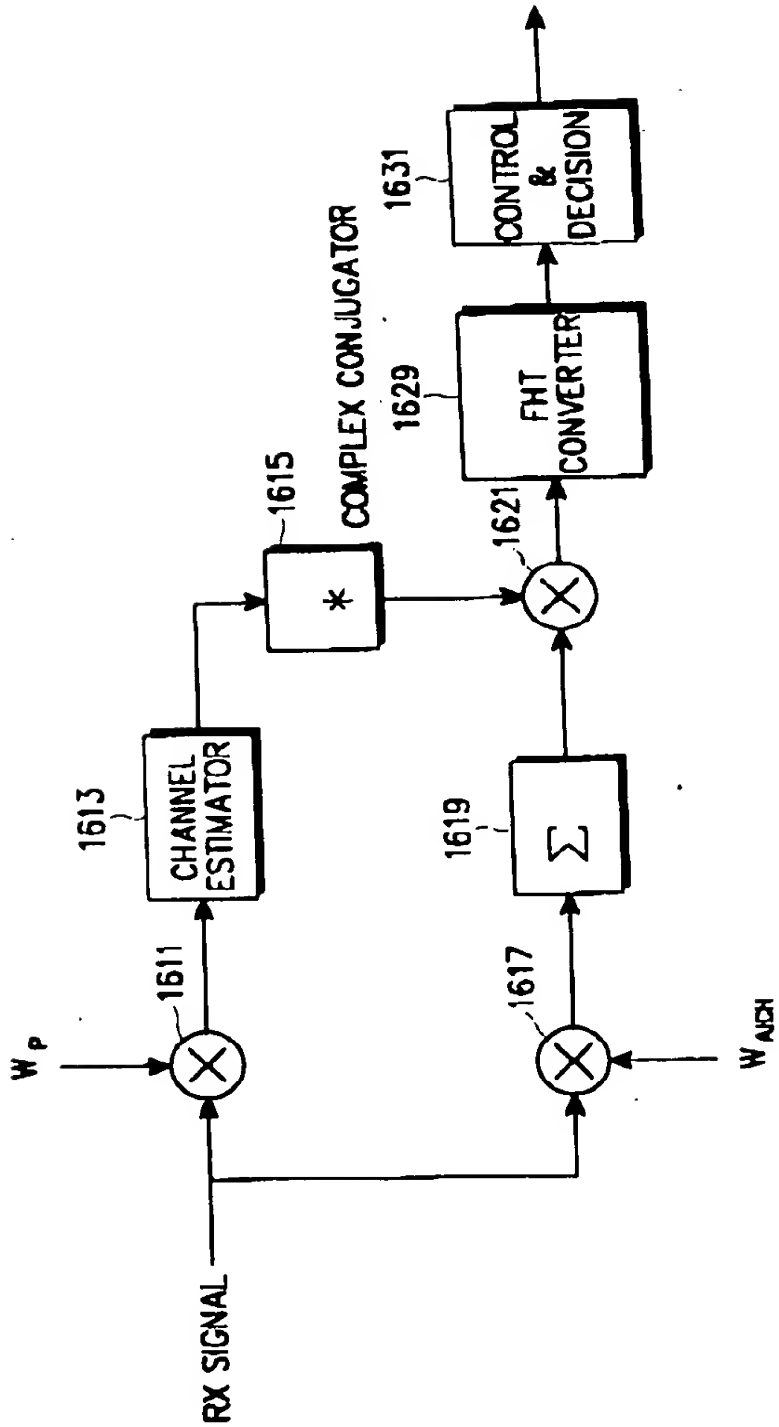
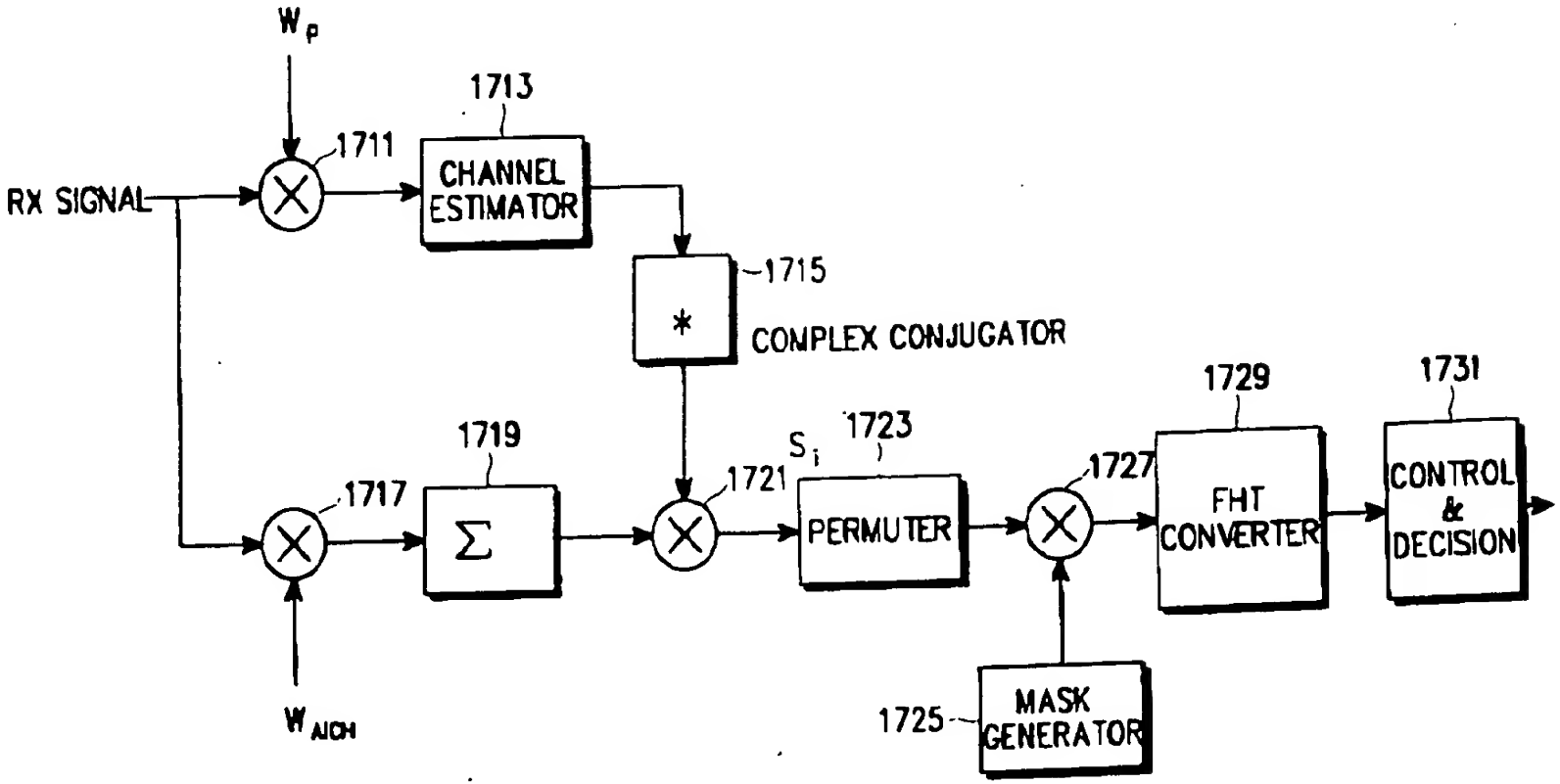

RX SIGNAL
W_P
1611
1613
CHANNEL ESTIMATOR
1615
COMPLEX CONJUGATOR
1617
W_AICH
1619
Σ
1621
1629
FHT CONVERTER
1631
CONTROL & DECISION

FIG. 17


W_P
1713
1711
RX SIGNAL
CHANNEL ESTIMATOR
1715
*
COMPLEX CONJUGATOR
1729
1731
1719
S_i
1723
1721
1727
1717
Σ
PERMUTER
FHT CONVERTER
CONTROL & DECISION
W_AICH
1725
MASK GENERATOR

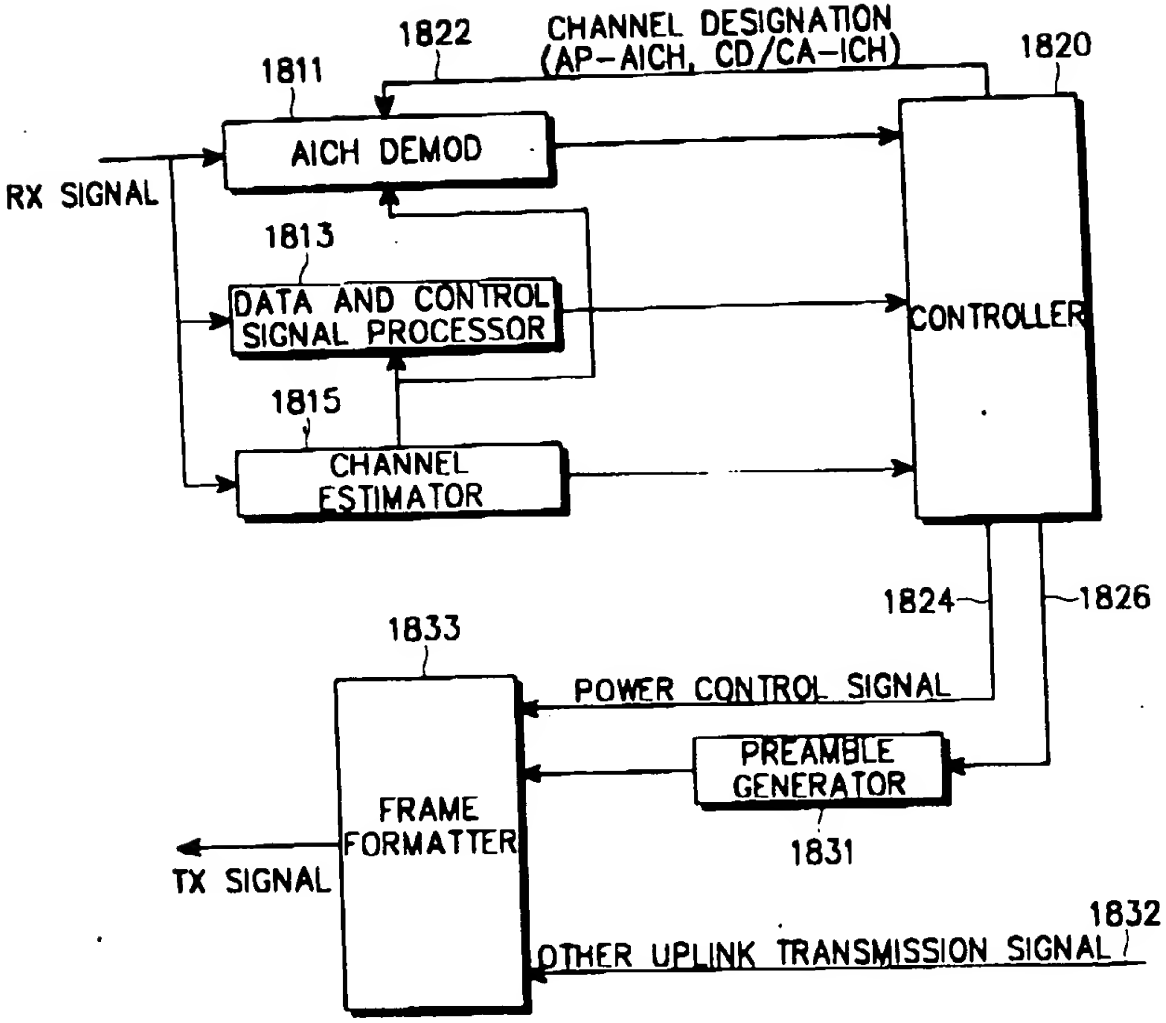

1822
CHANNEL DESIGNATION
(AP-AICH, CD/CA-ICH)
1820
1811
AICH DEMOD
RX SIGNAL
1813
DATA AND CONTROL
SIGNAL PROCESSOR
CONTROLLER
1815
CHANNEL
ESTIMATOR
1824
1826
1833
POWER CONTROL SIGNAL
PREAMBLE
GENERATOR
FRAME
FORMATTER
1831
TX SIGNAL
1832
OTHER UPLINK TRANSMISSION SIGNAL

FIG. 18

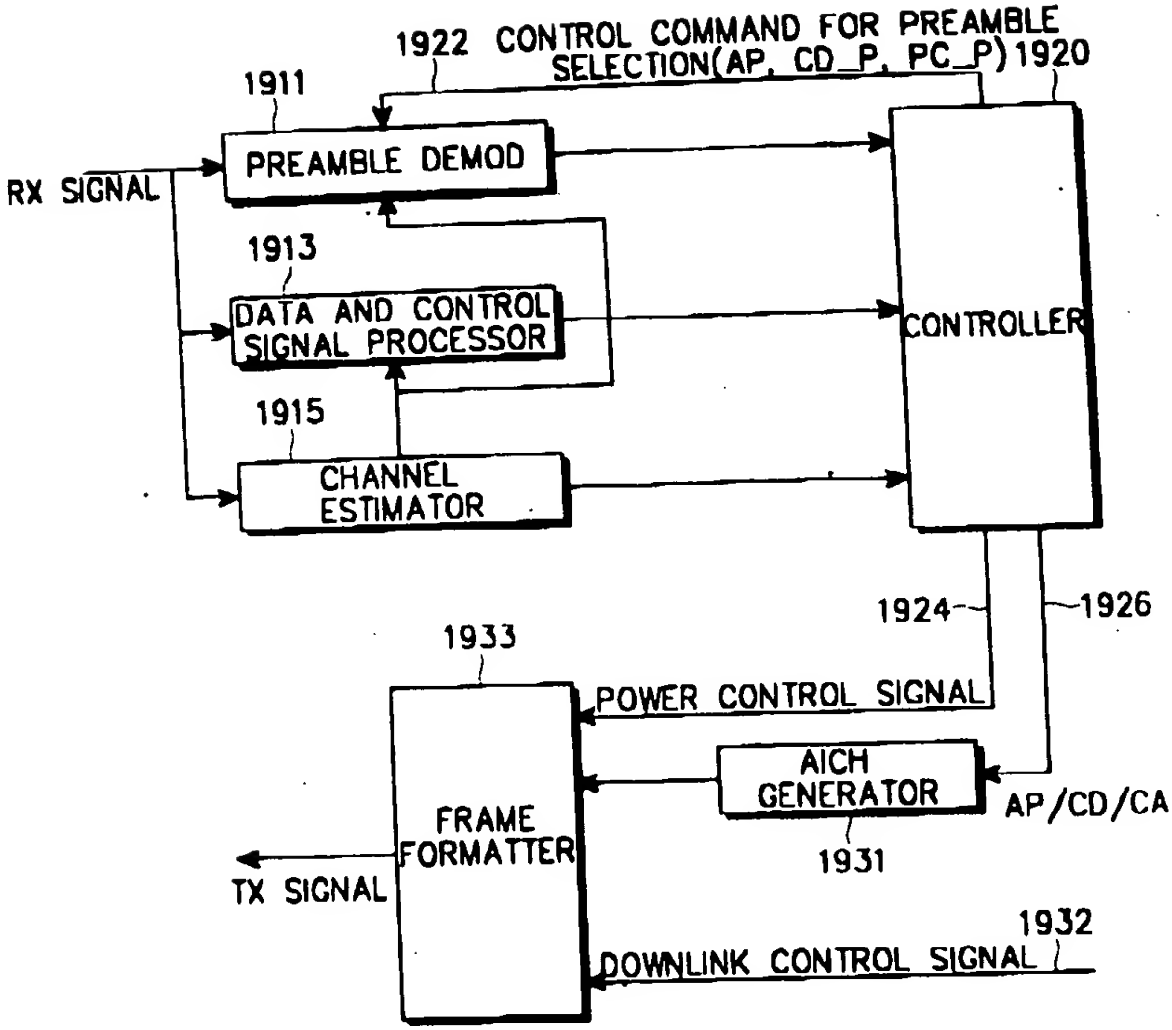

1922 CONTROL COMMAND FOR PREAMBLE SELECTION(AP, CD_P, PC_P) 1920
1911
PREAMBLE DEMOD
RX SIGNAL
1913
DATA AND CONTROL SIGNAL PROCESSOR
CONTROLLER
1915
CHANNEL ESTIMATOR
1924
1926
1933
POWER CONTROL SIGNAL
AICH GENERATOR
AP/CD/CA
FRAME FORMATTER
1931
TX SIGNAL
1932
DOWNLINK CONTROL SIGNAL

FIG. 19

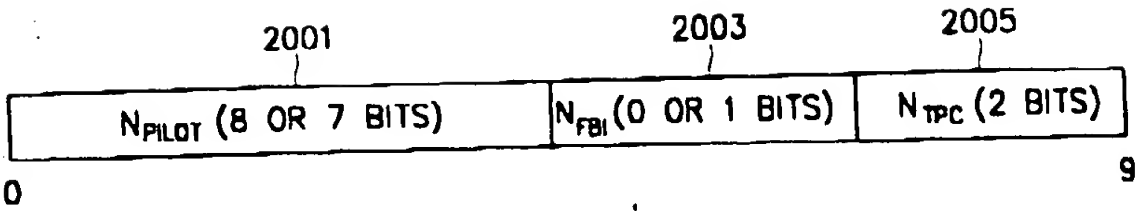


FIG. 20

09/503,689

FIG. 21

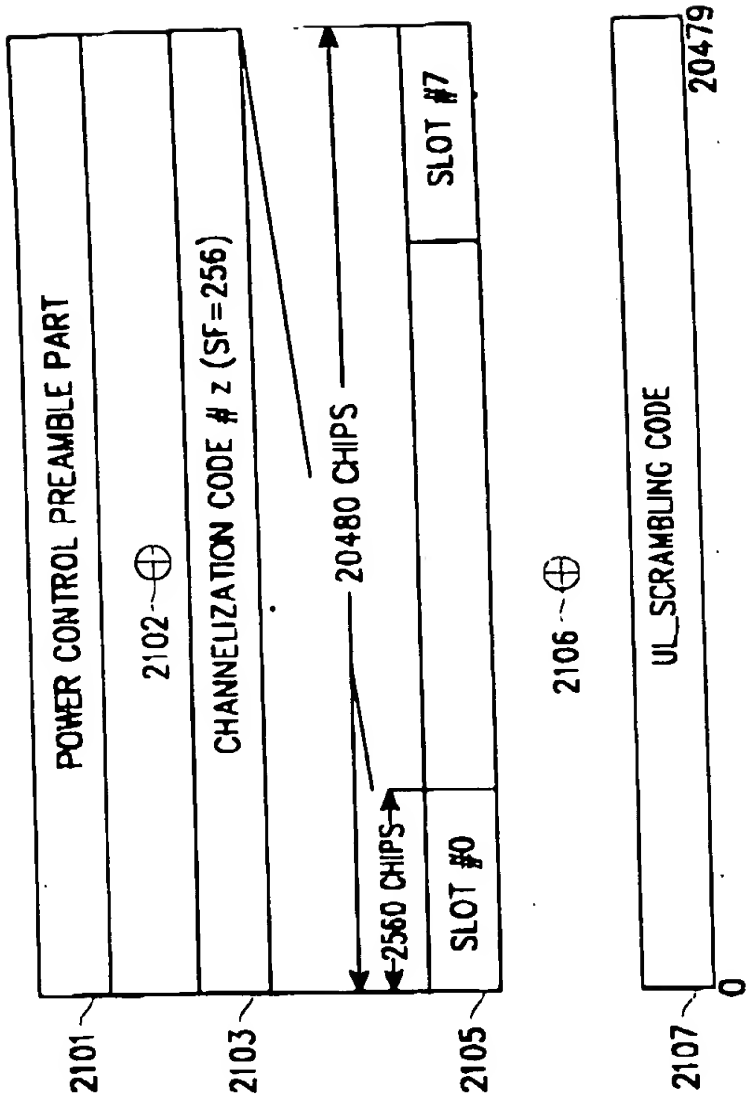

POWER CONTROL PREAMBLE PART
2102
CHANNELIZATION CODE # z (SF=256)
20480 CHIPS
SLOT #7
2560 CHIPS
SLOT #0
2106
UL_SCRAMBLING CODE
20479
0
2101
2103
2105
2107

FIG. 22A

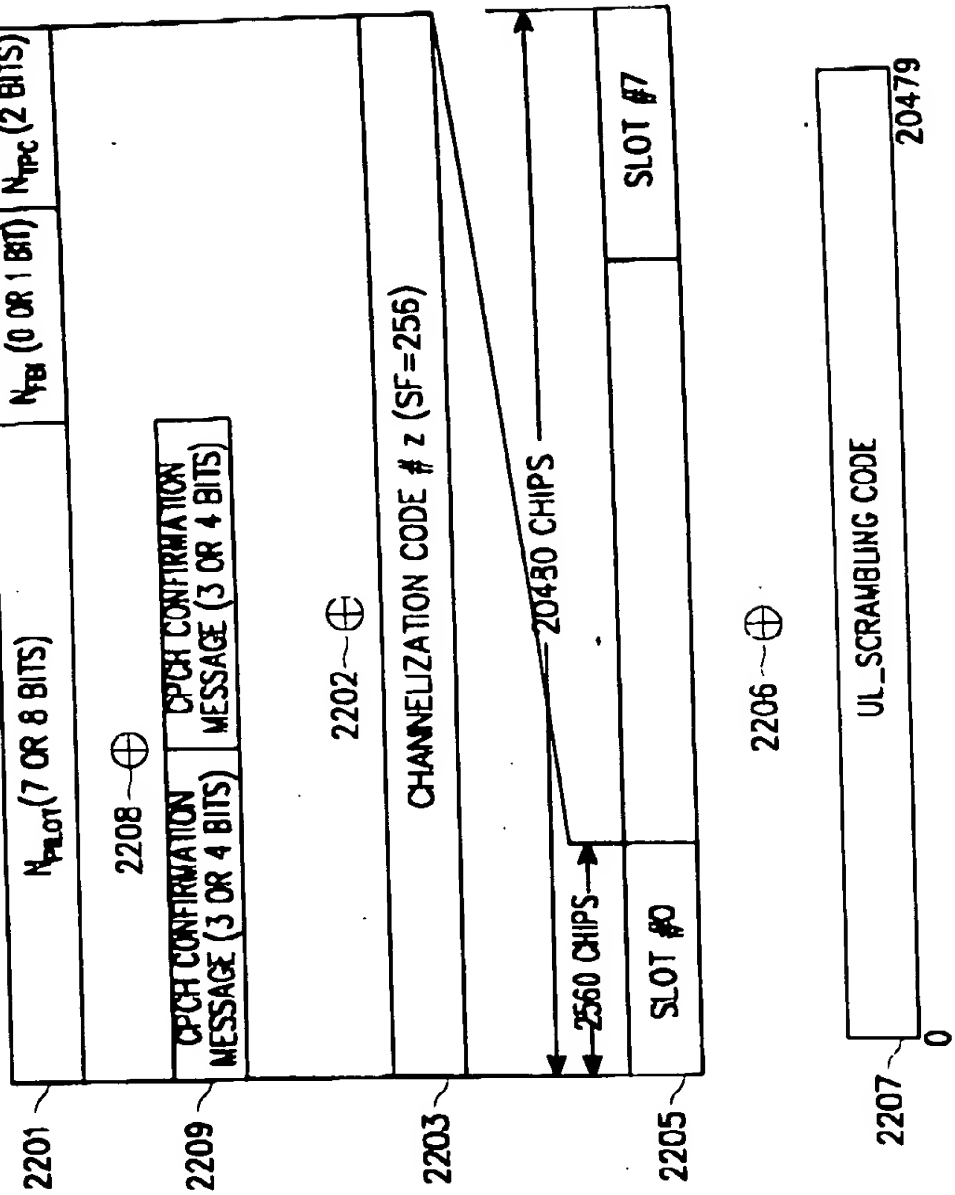

N_{PILOT}(7 OR 8 BITS)
N_{TFI} (0 OR 1 BIT)
N_{TPC} (2 BITS)
2208
OPCH CONFIRMATION MESSAGE (3 OR 4 BITS)
OPCH CONFIRMATION MESSAGE (3 OR 4 BITS)
2202
CHANNELIZATION CODE # z (SF=256)
20480 CHIPS
2560 CHIPS
SLOT #0
SLOT #7
2206
UL_SCRAMBLING CODE
20479
0
2201
2209
2203
2205
2207

FIG. 22B

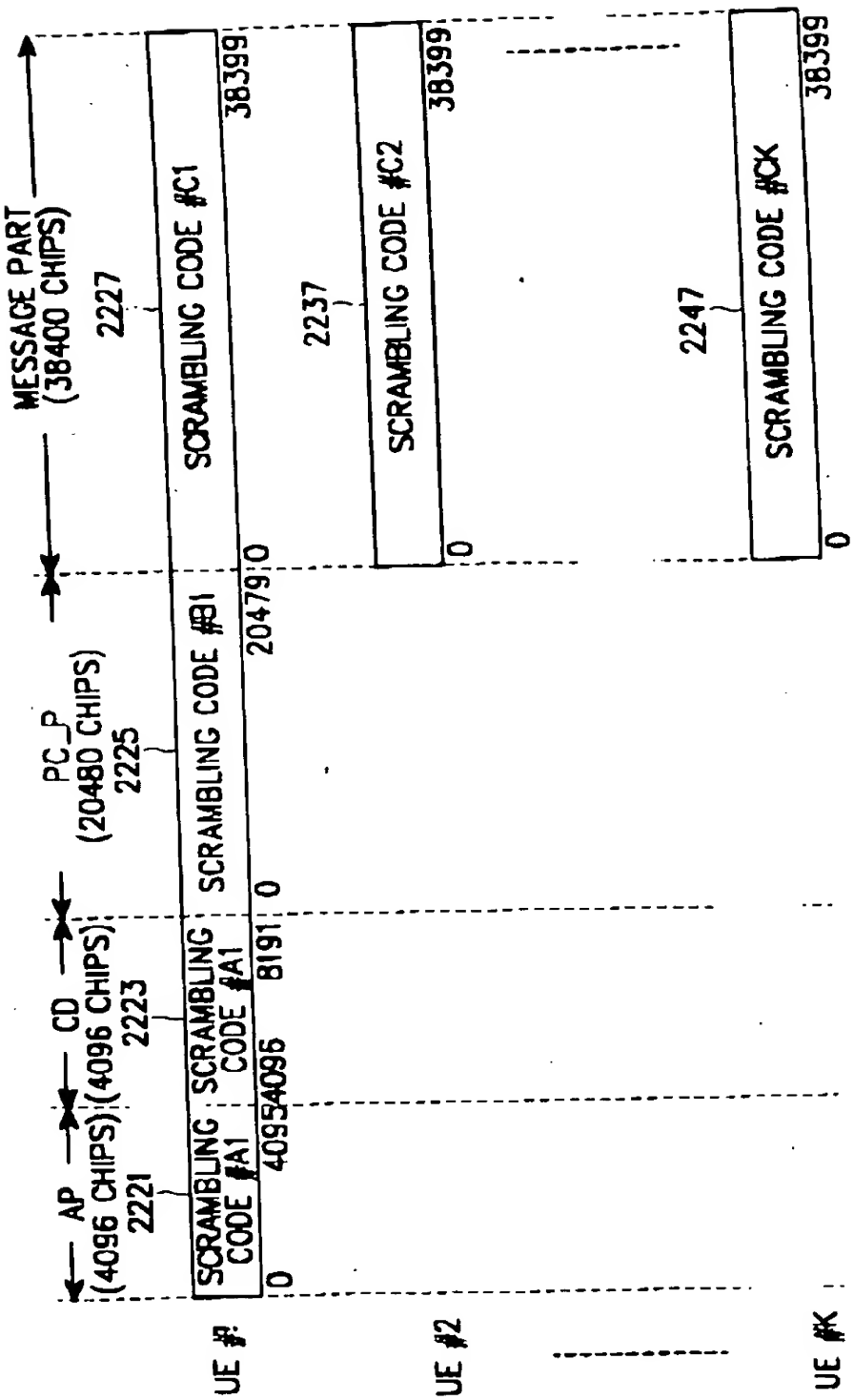

UE #1
UE #2
UE #K
AP (4096 CHIPS) 2221
CD (4096 CHIPS) 2223
PC_P (20480 CHIPS) 2225
MESSAGE PART (38400 CHIPS)
2227
2237
2247
SCRAMBLING CODE #A1
SCRAMBLING CODE #B1
SCRAMBLING CODE #C1
SCRAMBLING CODE #C2
SCRAMBLING CODE #CK
0
4095
4096
8191
20479
38399

FIG. 23

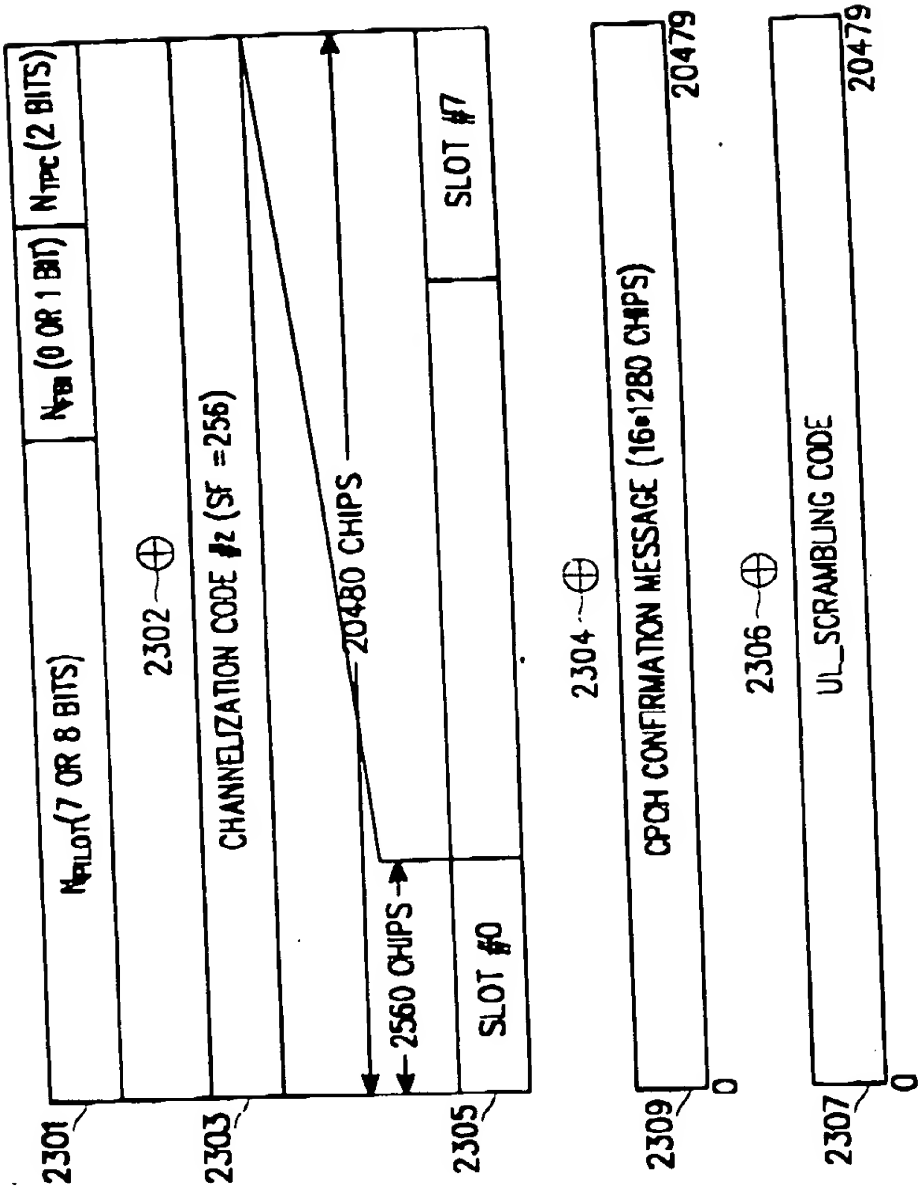

N_{PILOT}(7 OR 8 BITS)
N_{TPC} (0 OR 1 BIT)
N_{TFCI} (2 BITS)
2302
CHANNELIZATION CODE #k (SF =256)
20480 CHIPS
2560 CHIPS
SLOT #0
SLOT #7
2301
2303
2305
2304
CPCH CONFIRMATION MESSAGE (16*1280 CHIPS)
20479
0
2309
2306
UL_SCRAMBLING CODE
20479
0
2307

FIG. 24A

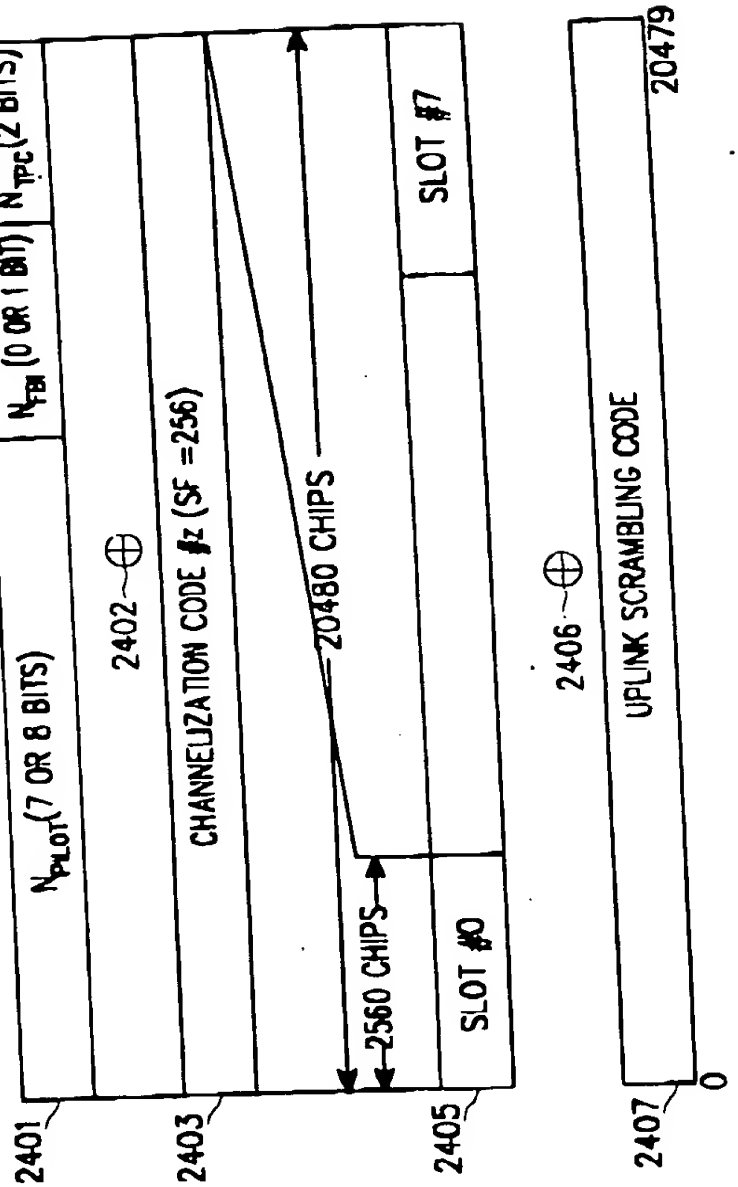

N_{PILOT}(7 OR 8 BITS)
N_{TFI} (0 OR 1 BIT)
N_{TPC}(2 BITS)
2402
CHANNELIZATION CODE #z (SF =256)
20480 CHIPS
2560 CHIPS
SLOT #0
SLOT #7
2401
2403
2405
2406
UPLINK SCRAMBLING CODE
20479
0
2407

FIG. 24B

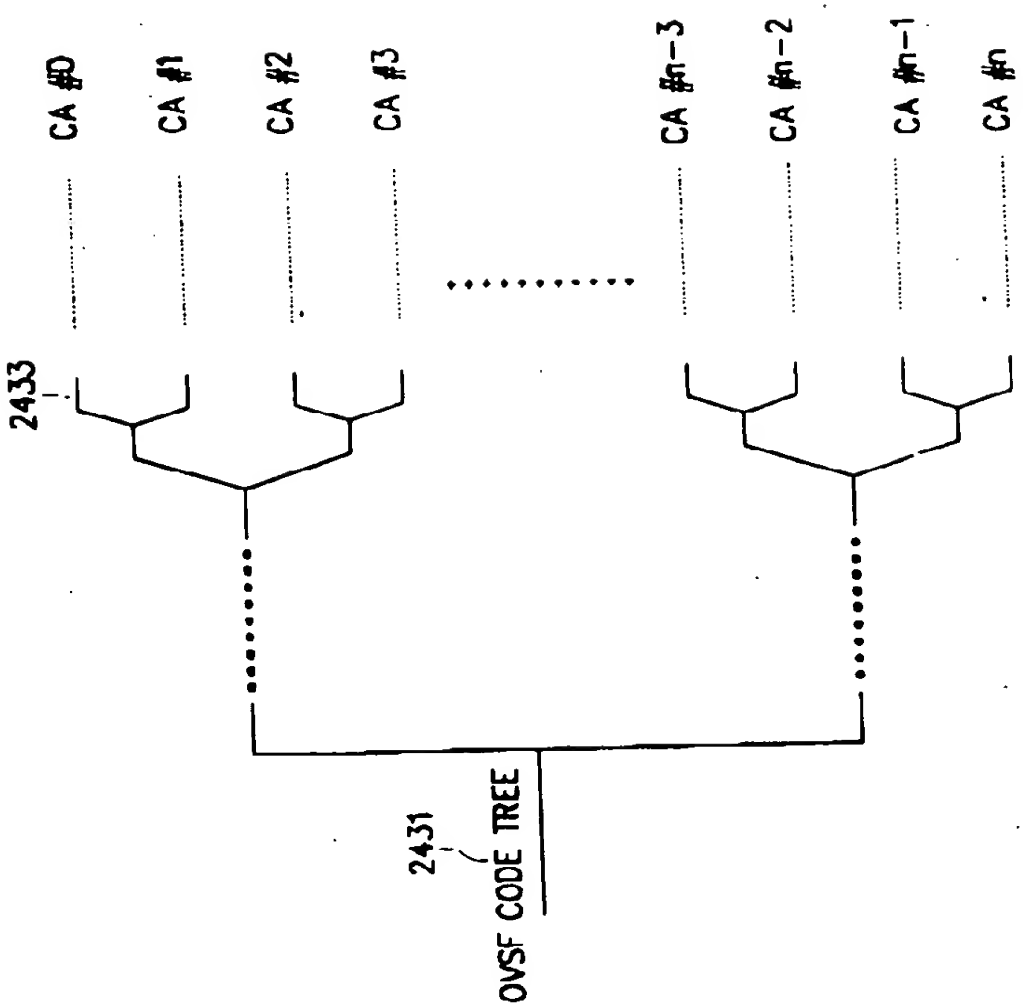


FIG. 25A

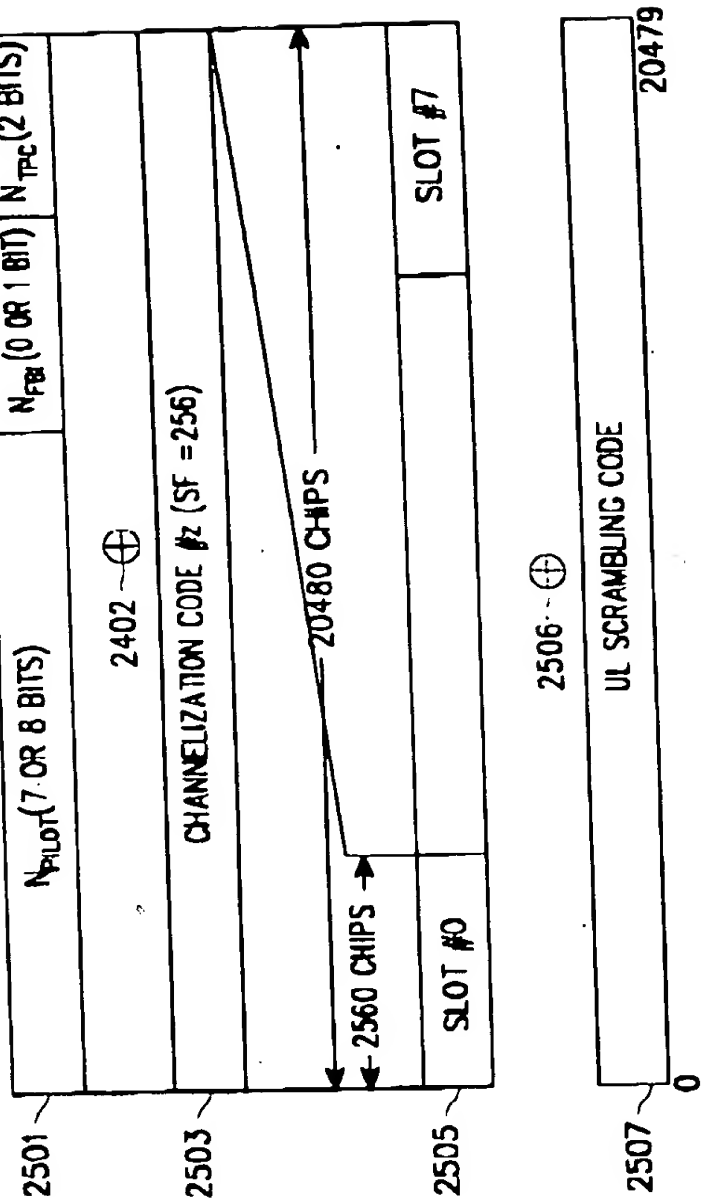

N_{PILOT}(7 OR 8 BITS)
N_{FBI}(0 OR 1 BIT)
N_{TPC}(2 BITS)
2402
CHANNELIZATION CODE #k (SF = 256)
20480 CHIPS
2560 CHIPS
SLOT #0
SLOT #7
2501
2503
2505
2506
UL SCRAMBLING CODE
20479
0
2507

FIG. 25B

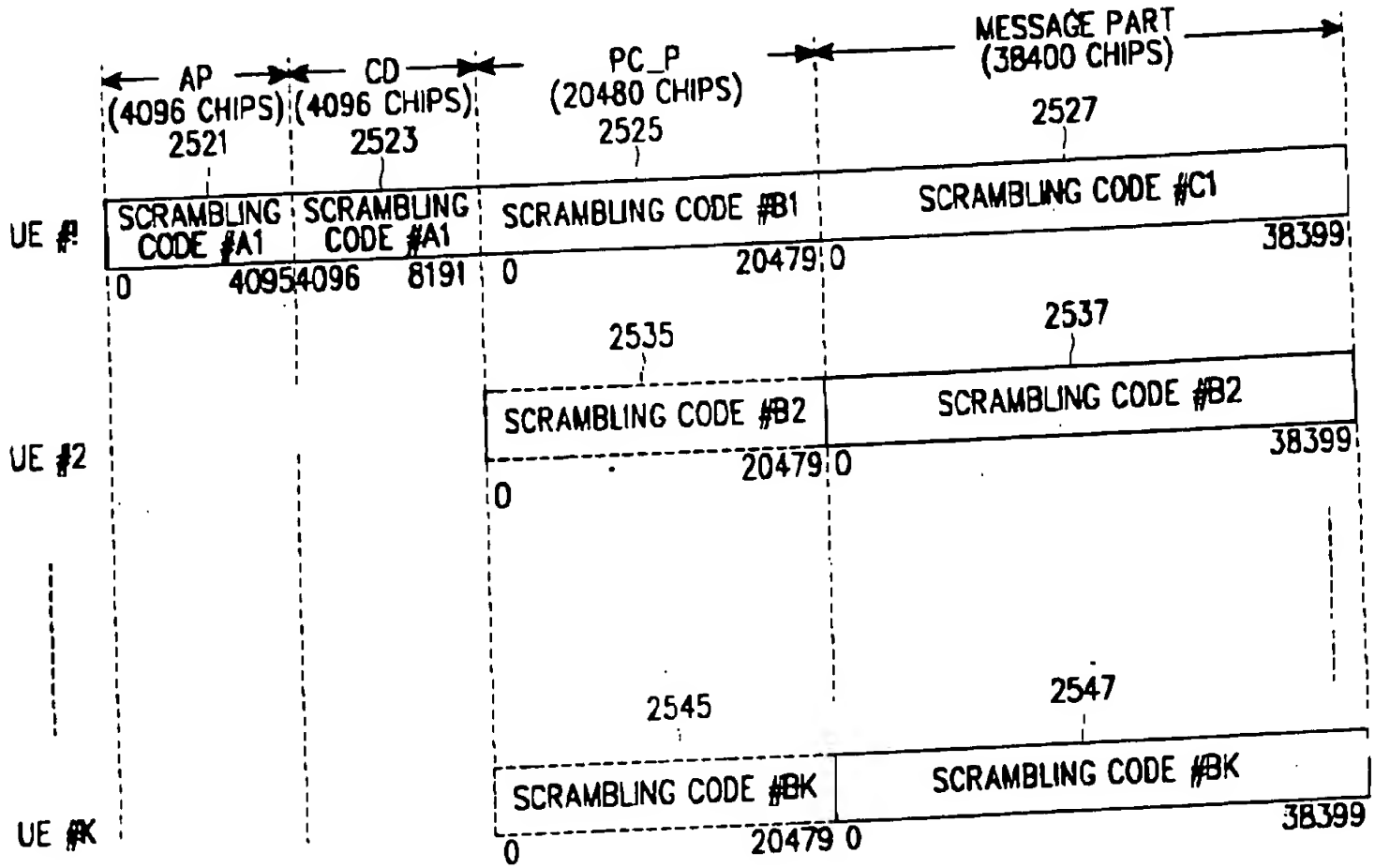
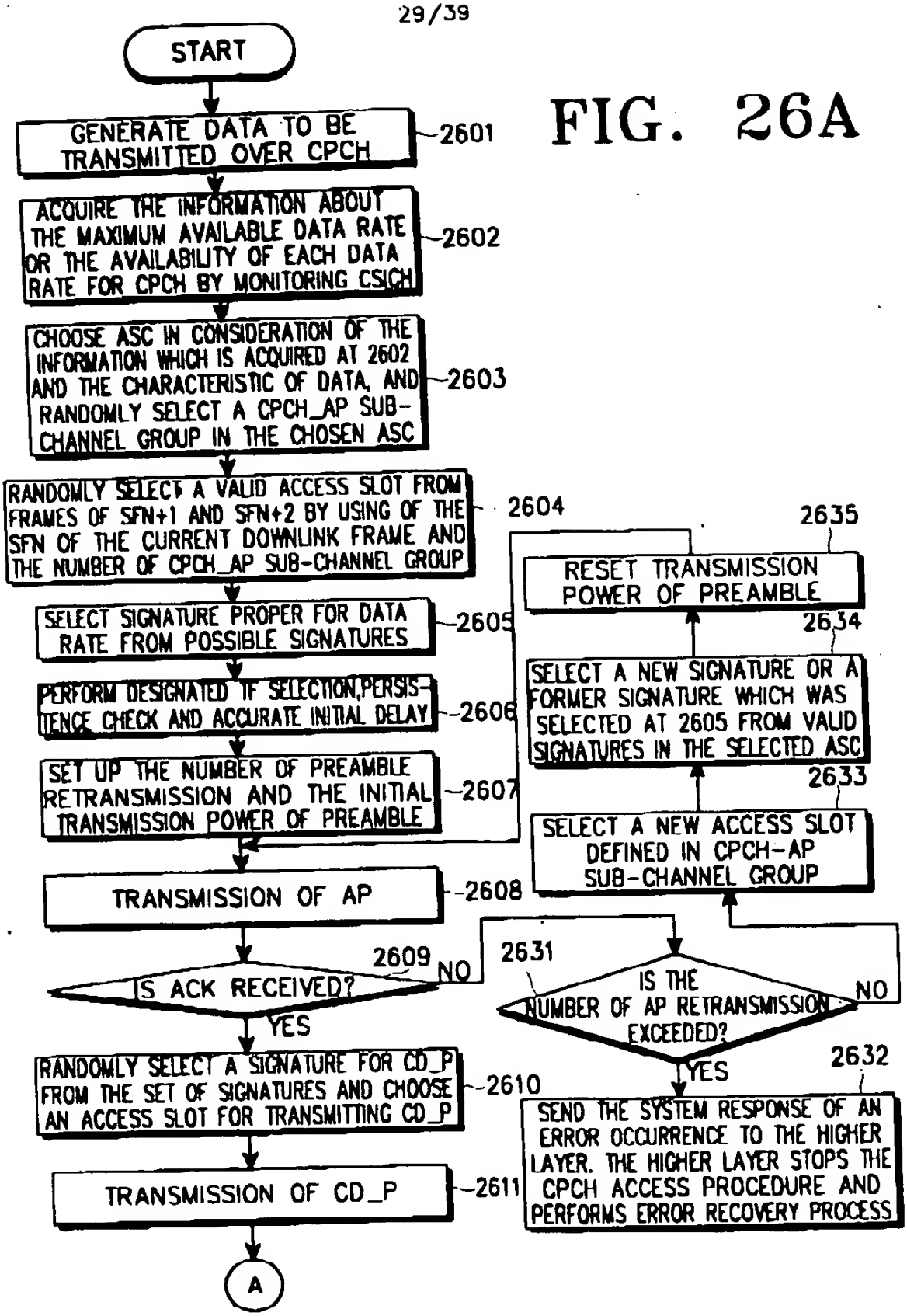

AP
(4096 CHIPS)
2521
CD
(4096 CHIPS)
2523
PC_P
(20480 CHIPS)
2525
MESSAGE PART
(38400 CHIPS)
2527
UE #1
SCRAMBLING CODE #A1
SCRAMBLING CODE #A1
SCRAMBLING CODE #B1
SCRAMBLING CODE #C1
0
4095
4096
8191
0
20479
0
38399
2535
2537
UE #2
SCRAMBLING CODE #B2
SCRAMBLING CODE #B2
0
20479
0
38399
2545
2547
UE #K
SCRAMBLING CODE #BK
SCRAMBLING CODE #BK
0
20479
0
38399

FIG. 26A


START
GENERATE DATA TO BE TRANSMITTED OVER CPCH
2601
ACQUIRE THE INFORMATION ABOUT THE MAXIMUM AVAILABLE DATA RATE OR THE AVAILABILITY OF EACH DATA RATE FOR CPCH BY MONITORING CSICH
2602
CHOOSE ASC IN CONSIDERATION OF THE INFORMATION WHICH IS ACQUIRED AT 2602 AND THE CHARACTERISTIC OF DATA, AND RANDOMLY SELECT A CPCH_AP SUB-CHANNEL GROUP IN THE CHOSEN ASC
2603
RANDOMLY SELECT A VALID ACCESS SLOT FROM FRAMES OF SFN+1 AND SFN+2 BY USING OF THE SFN OF THE CURRENT DOWNLINK FRAME AND THE NUMBER OF CPCH_AP SUB-CHANNEL GROUP
2604
SELECT SIGNATURE PROPER FOR DATA RATE FROM POSSIBLE SIGNATURES
2605
PERFORM DESIGNATED TF SELECTION, PERSISTENCE CHECK AND ACCURATE INITIAL DELAY
2606
SET UP THE NUMBER OF PREAMBLE RETRANSMISSION AND THE INITIAL TRANSMISSION POWER OF PREAMBLE
2607
TRANSMISSION OF AP
2608
IS ACK RECEIVED?
2609
NO
YES
RANDOMLY SELECT A SIGNATURE FOR CD_P FROM THE SET OF SIGNATURES AND CHOOSE AN ACCESS SLOT FOR TRANSMITTING CD_P
2610
TRANSMISSION OF CD_P
2611
A
IS THE NUMBER OF AP RETRANSMISSION EXCEEDED?
2631
NO
YES
SEND THE SYSTEM RESPONSE OF AN ERROR OCCURRENCE TO THE HIGHER LAYER. THE HIGHER LAYER STOPS THE CPCH ACCESS PROCEDURE AND PERFORMS ERROR RECOVERY PROCESS
2632
SELECT A NEW ACCESS SLOT DEFINED IN CPCH-AP SUB-CHANNEL GROUP
2633
SELECT A NEW SIGNATURE OR A FORMER SIGNATURE WHICH WAS SELECTED AT 2605 FROM VALID SIGNATURES IN THE SELECTED ASC
2634
RESET TRANSMISSION POWER OF PREAMBLE
2635

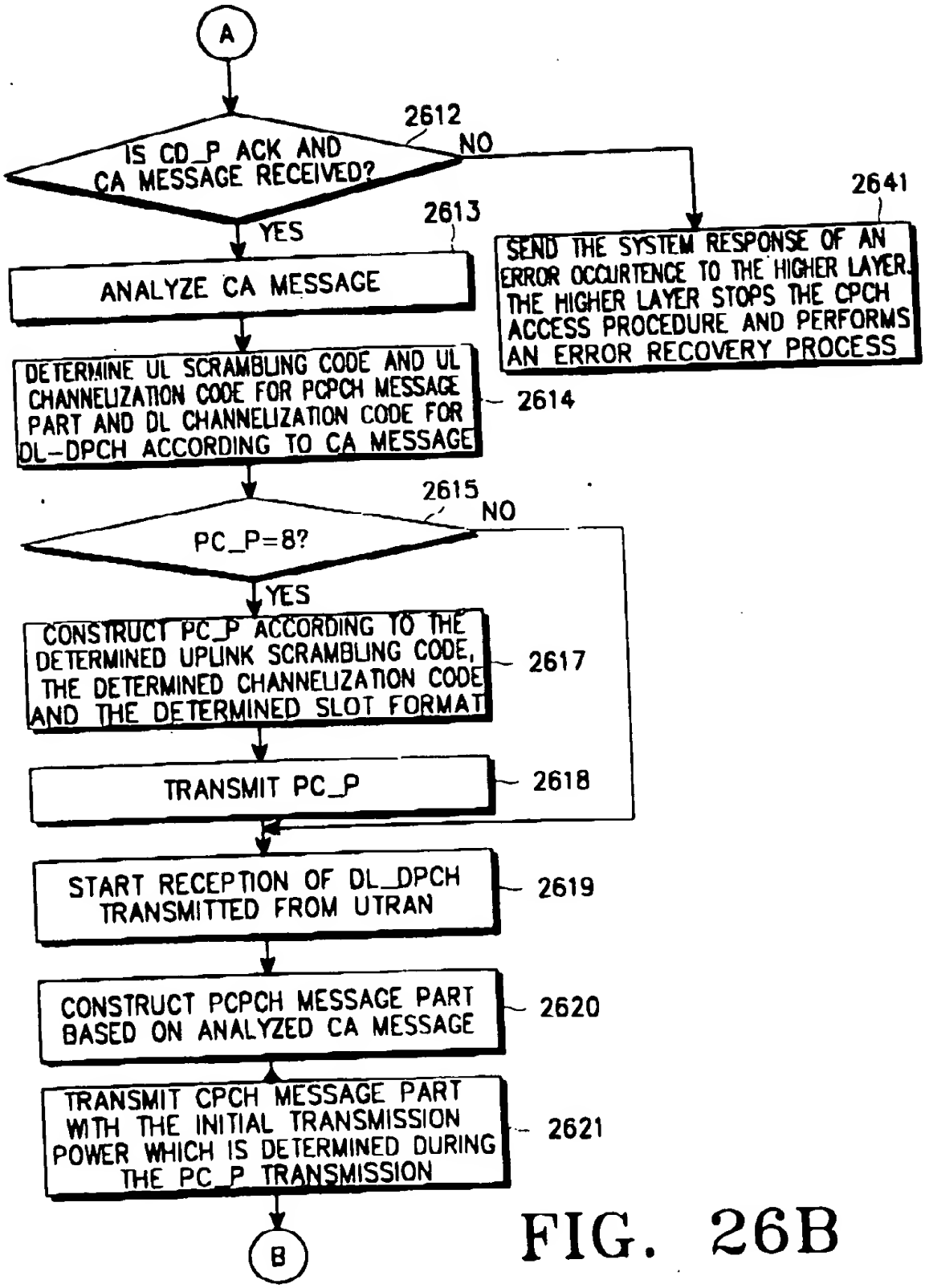

A
2612
IS CD_P ACK AND CA MESSAGE RECEIVED?
NO
YES
2641
SEND THE SYSTEM RESPONSE OF AN ERROR OCCURTENCE TO THE HIGHER LAYER. THE HIGHER LAYER STOPS THE CPCH ACCESS PROCEDURE AND PERFORMS AN ERROR RECOVERY PROCESS
2613
ANALYZE CA MESSAGE
DETERMINE UL SCRAMBLING CODE AND UL CHANNELIZATION CODE FOR PCPCH MESSAGE PART AND DL CHANNELIZATION CODE FOR DL-DPCH ACCORDING TO CA MESSAGE
2614
2615
PC_P=8?
NO
YES
CONSTRUCT PC_P ACCORDING TO THE DETERMINED UPLINK SCRAMBLING CODE, THE DETERMINED CHANNELIZATION CODE AND THE DETERMINED SLOT FORMAT
2617
TRANSMIT PC_P
2618
START RECEPTION OF DL_DPCH TRANSMITTED FROM UTRAN
2619
CONSTRUCT PCPCH MESSAGE PART BASED ON ANALYZED CA MESSAGE
2620
TRANSMIT CPCH MESSAGE PART WITH THE INITIAL TRANSMISSION POWER WHICH IS DETERMINED DURING THE PC_P TRANSMISSION
2621
B

FIG. 26B

FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT (UTRAN SIDE)

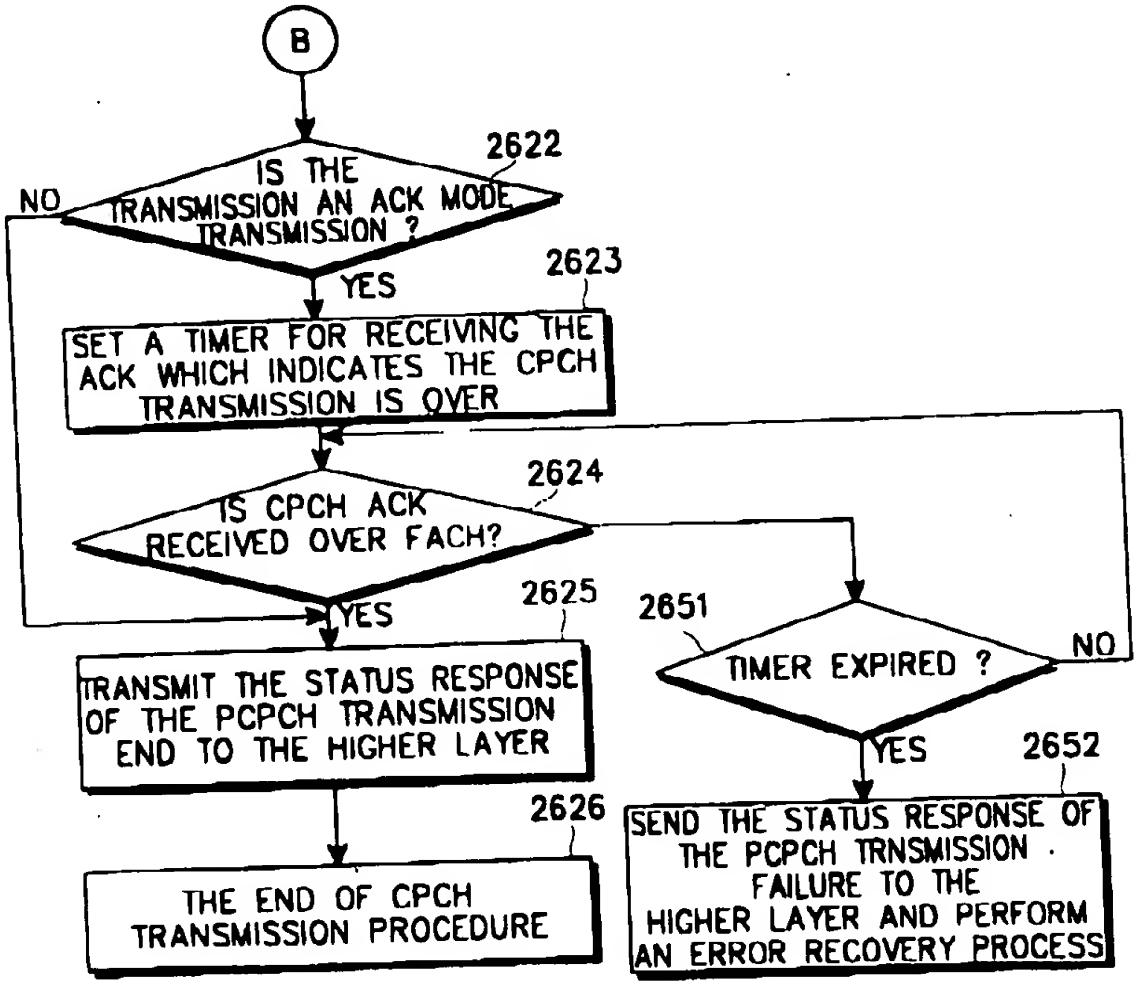


FIG. 26C

FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT (UTRAN SIDE)

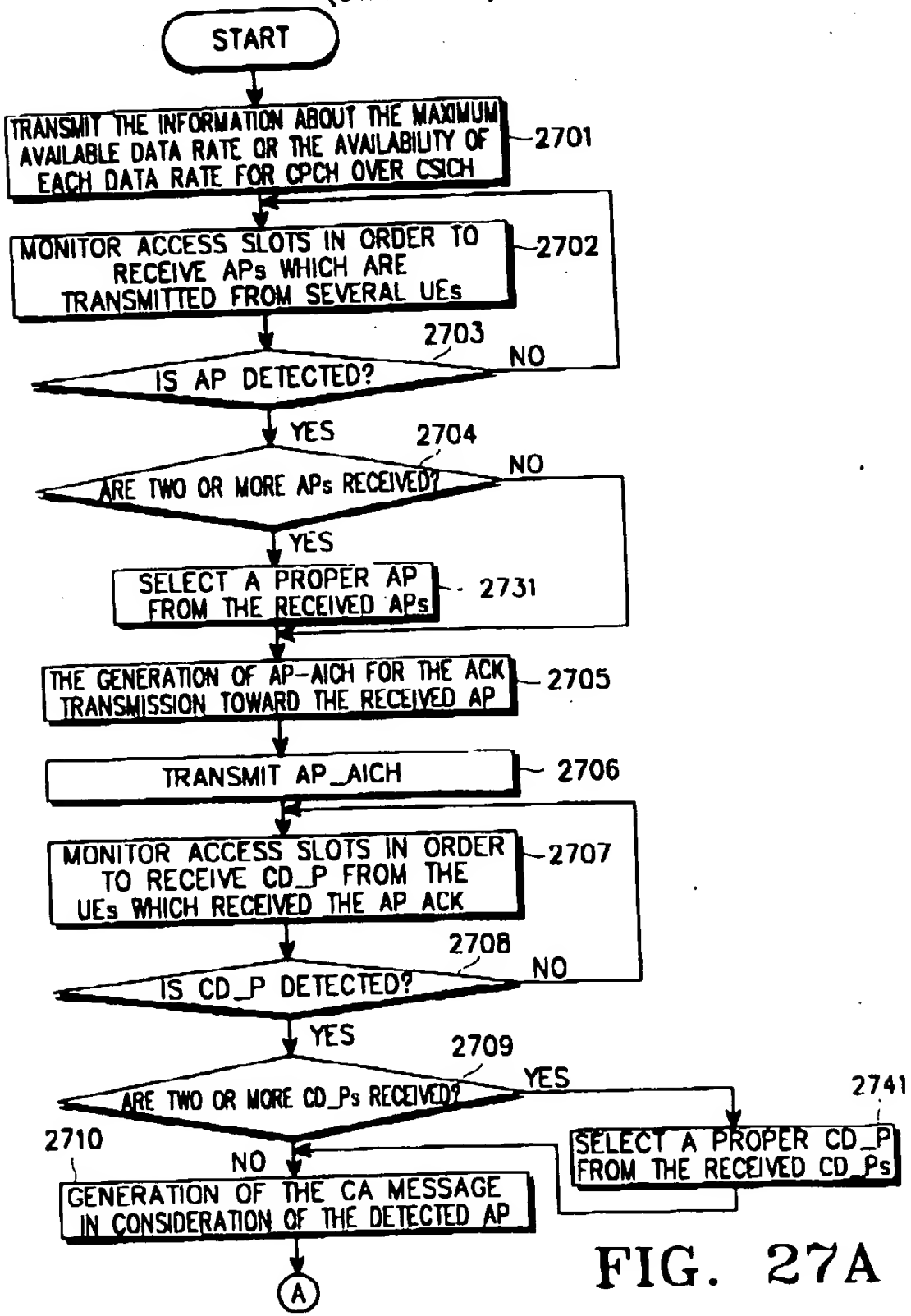


FIG. 27A

FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT (UTRAN SIDE)

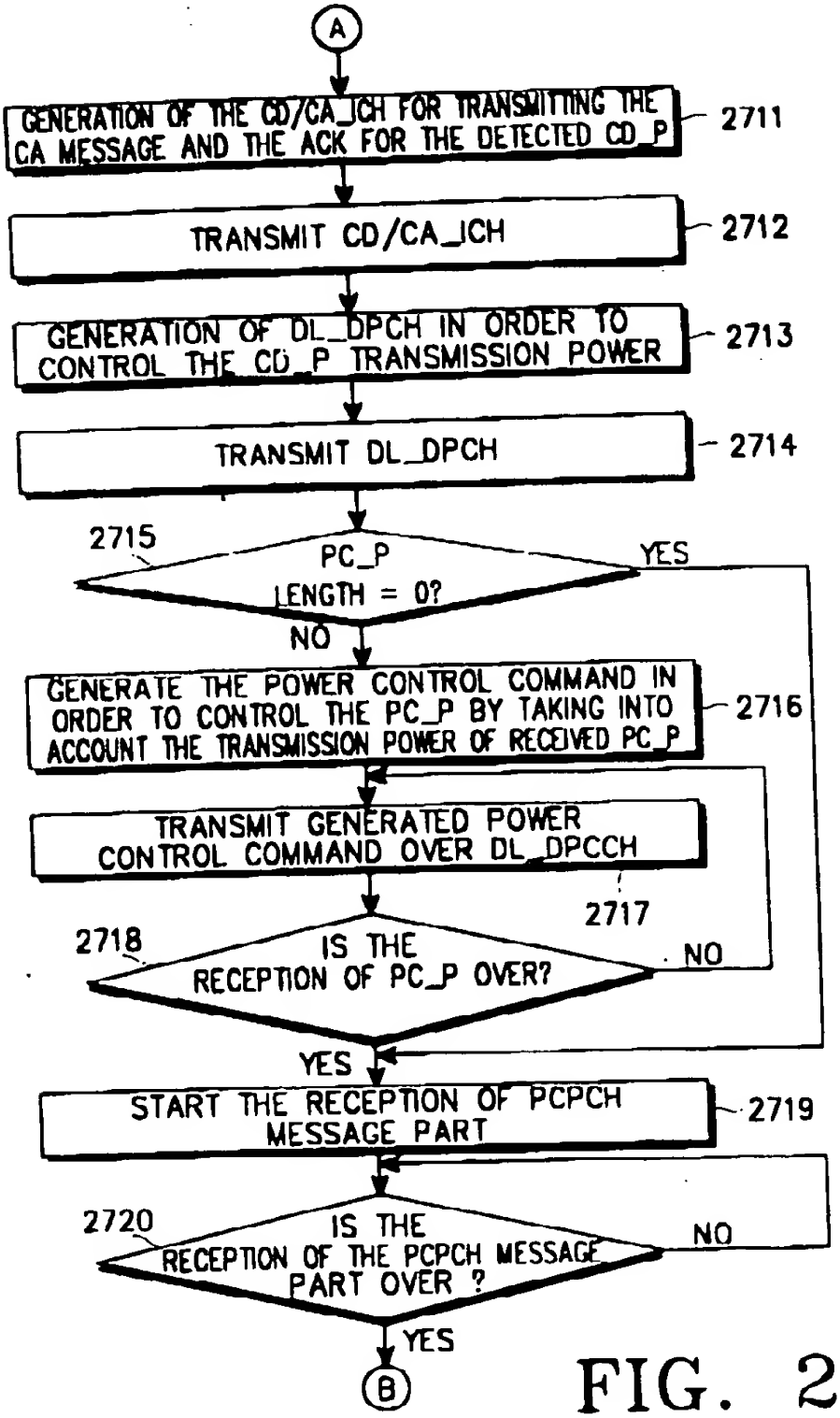


FIG. 27B

FLOWCHART OF CPCH USING CHANNEL ASSIGNMENT (UTRAN SIDE)

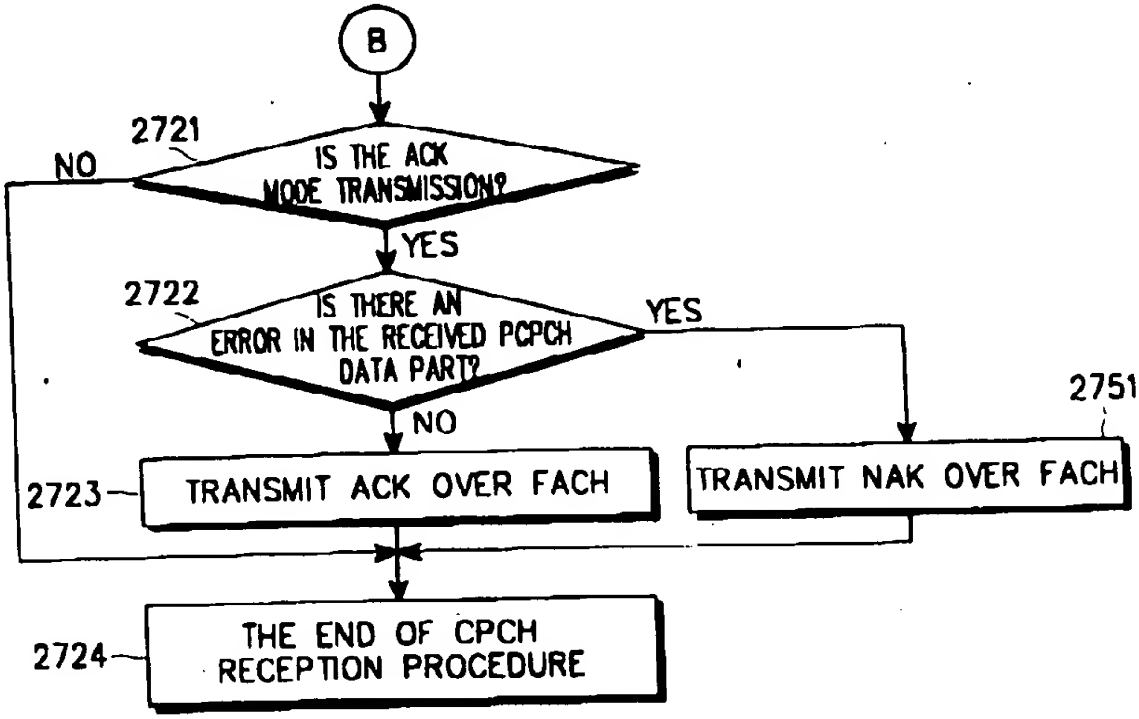


FIG. 27C

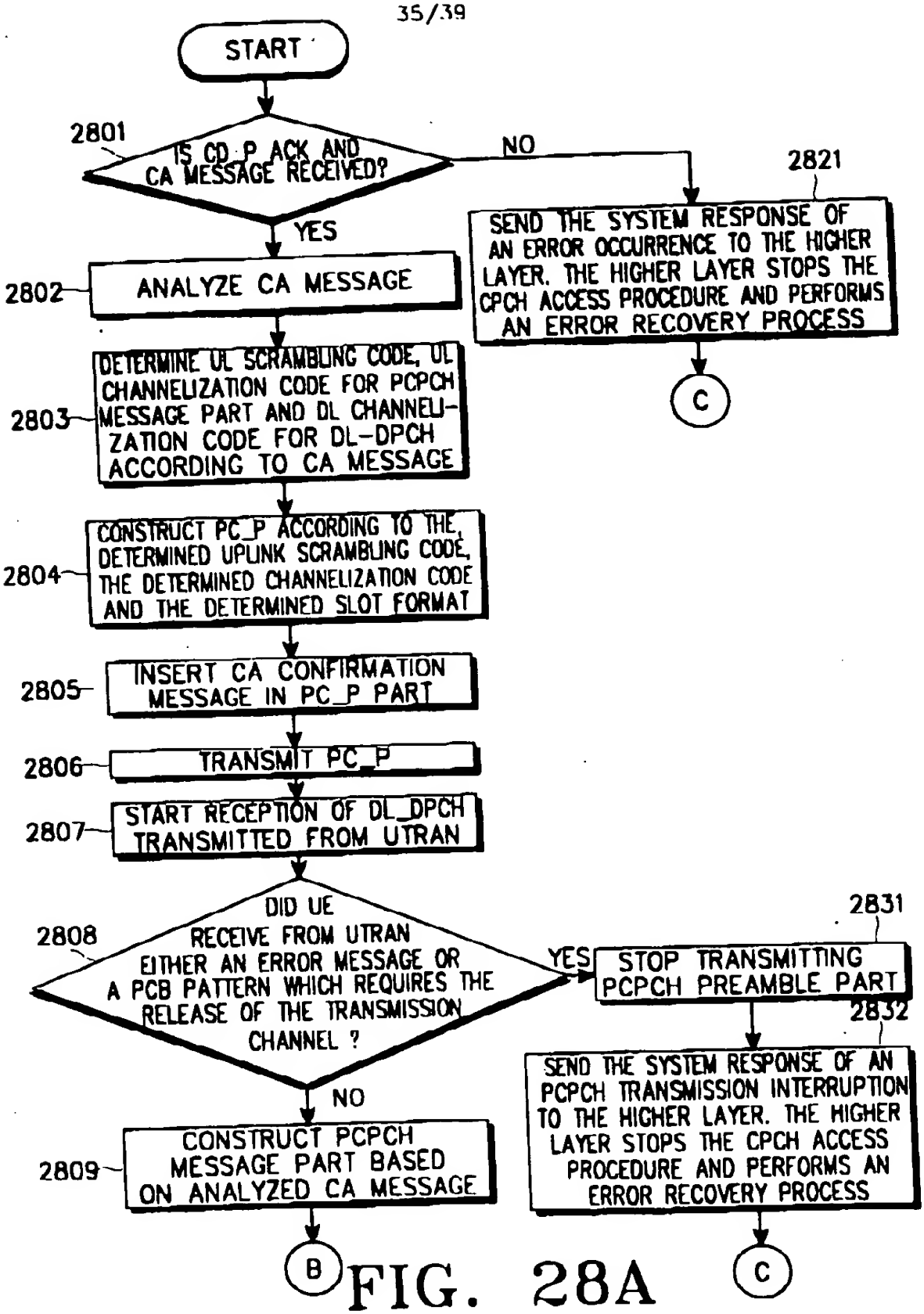

START
2801
IS CD_P ACK AND CA MESSAGE RECEIVED?
NO
2821
SEND THE SYSTEM RESPONSE OF AN ERROR OCCURRENCE TO THE HIGHER LAYER. THE HIGHER LAYER STOPS THE CPCH ACCESS PROCEDURE AND PERFORMS AN ERROR RECOVERY PROCESS
C
YES
2802
ANALYZE CA MESSAGE
2803
DETERMINE UL SCRAMBLING CODE, UL CHANNELIZATION CODE FOR PCPCH MESSAGE PART AND DL CHANNELIZATION CODE FOR DL-DPCH ACCORDING TO CA MESSAGE
2804
CONSTRUCT PC_P ACCORDING TO THE DETERMINED UPLINK SCRAMBLING CODE, THE DETERMINED CHANNELIZATION CODE AND THE DETERMINED SLOT FORMAT
2805
INSERT CA CONFIRMATION MESSAGE IN PC_P PART
2806
TRANSMIT PC_P
2807
START RECEPTION OF DL_DPCH TRANSMITTED FROM UTRAN
2808
DID UE RECEIVE FROM UTRAN EITHER AN ERROR MESSAGE OR A PCB PATTERN WHICH REQUIRES THE RELEASE OF THE TRANSMISSION CHANNEL ?
YES
2831
STOP TRANSMITTING PCPCH PREAMBLE PART
2832
SEND THE SYSTEM RESPONSE OF AN PCPCH TRANSMISSION INTERRUPTION TO THE HIGHER LAYER. THE HIGHER LAYER STOPS THE CPCH ACCESS PROCEDURE AND PERFORMS AN ERROR RECOVERY PROCESS
C
NO
2809
CONSTRUCT PCPCH MESSAGE PART BASED ON ANALYZED CA MESSAGE
B

FIG. 28A

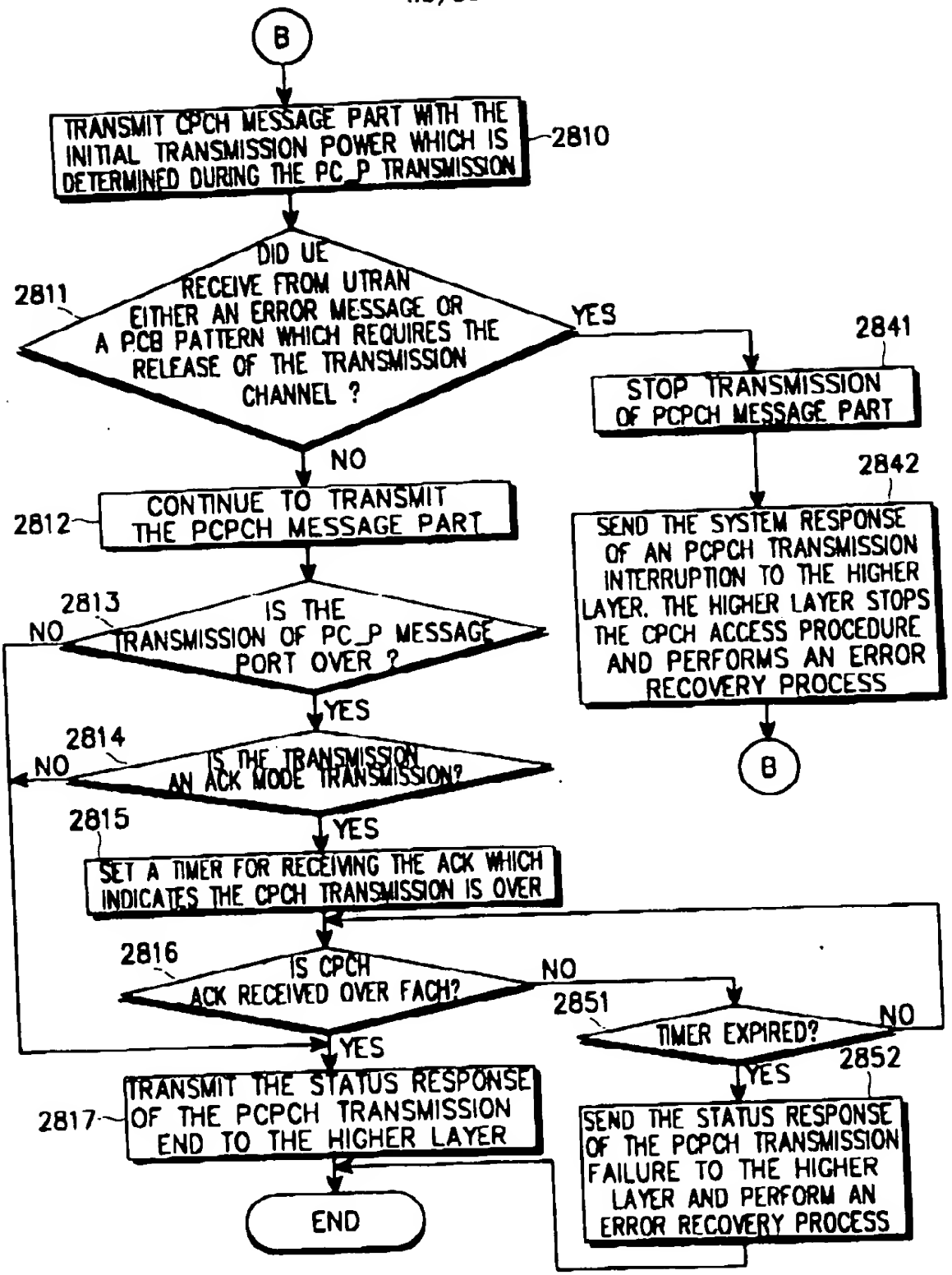

B
TRANSMIT CPCH MESSAGE PART WITH THE INITIAL TRANSMISSION POWER WHICH IS DETERMINED DURING THE PC_P TRANSMISSION
2810
DID UE RECEIVE FROM UTRAN EITHER AN ERROR MESSAGE OR A PCB PATTERN WHICH REQUIRES THE RELEASE OF THE TRANSMISSION CHANNEL ?
2811
YES
NO
2841
STOP TRANSMISSION OF PCPCH MESSAGE PART
2842
SEND THE SYSTEM RESPONSE OF AN PCPCH TRANSMISSION INTERRUPTION TO THE HIGHER LAYER. THE HIGHER LAYER STOPS THE CPCH ACCESS PROCEDURE AND PERFORMS AN ERROR RECOVERY PROCESS
B
2812
CONTINUE TO TRANSMIT THE PCPCH MESSAGE PART
2813
IS THE TRANSMISSION OF PC_P MESSAGE PORT OVER ?
NO
YES
2814
IS THE TRANSMISSION AN ACK MODE TRANSMISSION?
NO
YES
2815
SET A TIMER FOR RECEIVING THE ACK WHICH INDICATES THE CPCH TRANSMISSION IS OVER
2816
IS CPCH ACK RECEIVED OVER FACH?
NO
YES
2851
TIMER EXPIRED?
NO
YES
2852
SEND THE STATUS RESPONSE OF THE PCPCH TRANSMISSION FAILURE TO THE HIGHER LAYER AND PERFORM AN ERROR RECOVERY PROCESS
2817
TRANSMIT THE STATUS RESPONSE OF THE PCPCH TRANSMISSION END TO THE HIGHER LAYER
END

FIG. 28B

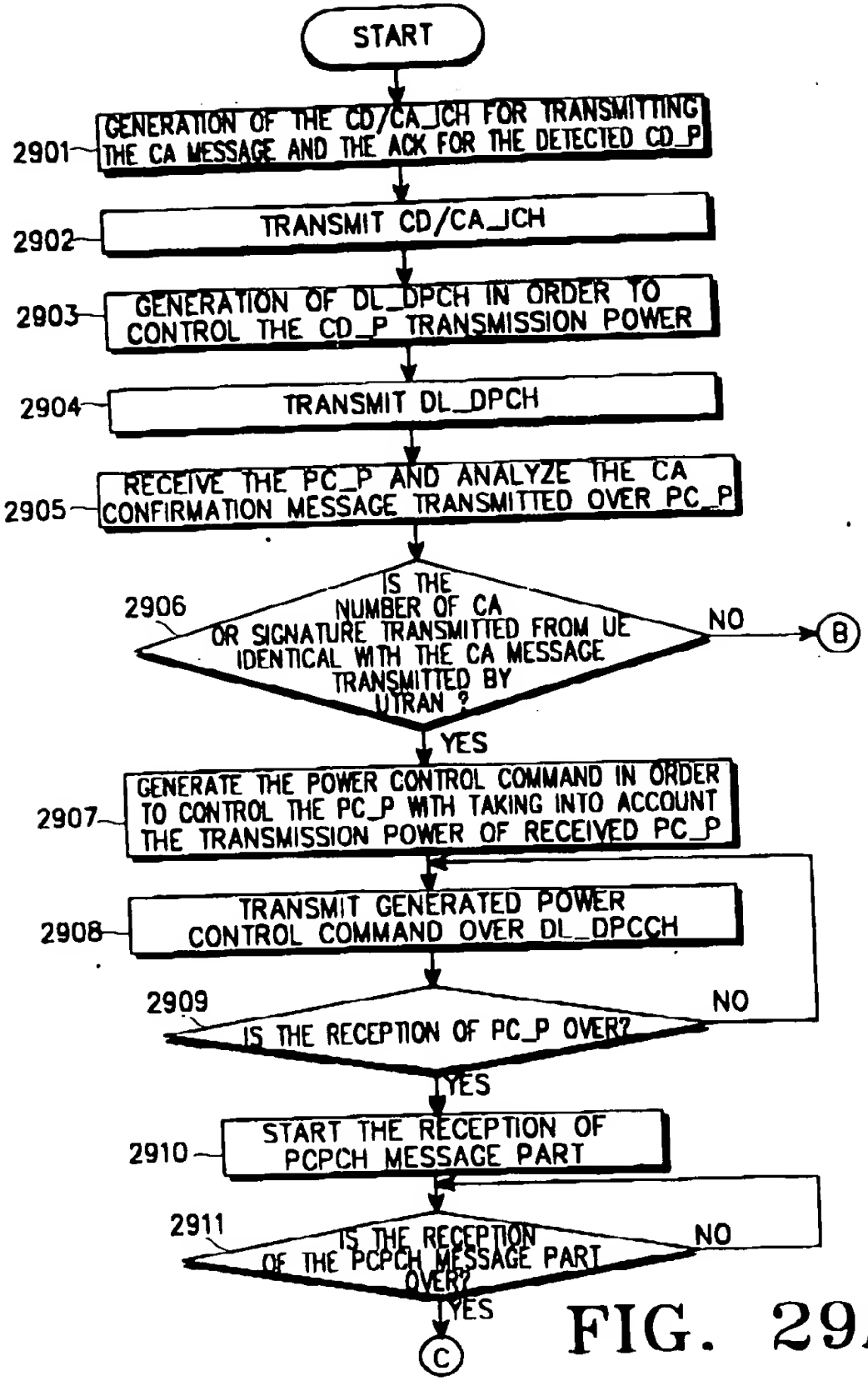

START
2901
GENERATION OF THE CD/CA_ICH FOR TRANSMITTING THE CA MESSAGE AND THE ACK FOR THE DETECTED CD_P
2902
TRANSMIT CD/CA_ICH
2903
GENERATION OF DL_DPCH IN ORDER TO CONTROL THE CD_P TRANSMISSION POWER
2904
TRANSMIT DL_DPCH
2905
RECEIVE THE PC_P AND ANALYZE THE CA CONFIRMATION MESSAGE TRANSMITTED OVER PC_P
2906
IS THE NUMBER OF CA OR SIGNATURE TRANSMITTED FROM UE IDENTICAL WITH THE CA MESSAGE TRANSMITTED BY UTRAN ?
NO
B
YES
2907
GENERATE THE POWER CONTROL COMMAND IN ORDER TO CONTROL THE PC_P WITH TAKING INTO ACCOUNT THE TRANSMISSION POWER OF RECEIVED PC_P
2908
TRANSMIT GENERATED POWER CONTROL COMMAND OVER DL_DPCCH
2909
IS THE RECEPTION OF PC_P OVER?
NO
YES
2910
START THE RECEPTION OF PCPCH MESSAGE PART
2911
IS THE RECEPTION OF THE PCPCH MESSAGE PART OVER?
NO
YES
C

FIG. 29A

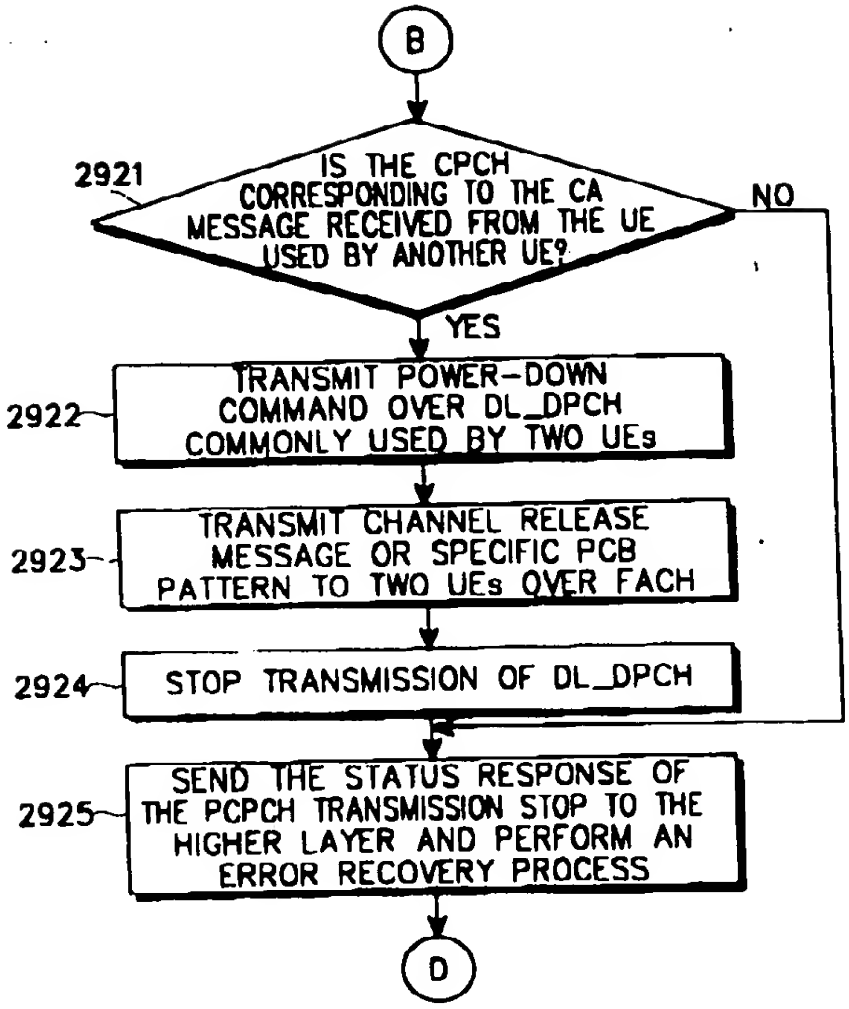

B
2921
IS THE CPCH CORRESPONDING TO THE CA MESSAGE RECEIVED FROM THE UE USED BY ANOTHER UE?
NO
YES
2922
TRANSMIT POWER-DOWN COMMAND OVER DL_DPCH COMMONLY USED BY TWO UEs
2923
TRANSMIT CHANNEL RELEASE MESSAGE OR SPECIFIC PCB PATTERN TO TWO UEs OVER FACH
2924
STOP TRANSMISSION OF DL_DPCH
2925
SEND THE STATUS RESPONSE OF THE PCPCH TRANSMISSION STOP TO THE HIGHER LAYER AND PERFORM AN ERROR RECOVERY PROCESS
D

FIG. 29B

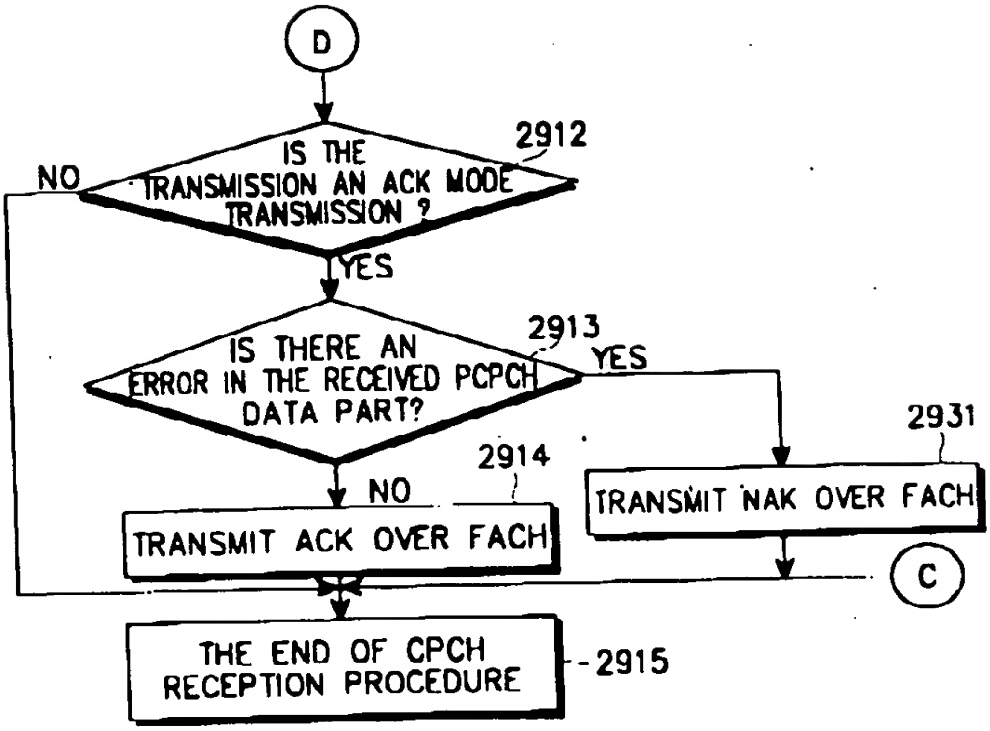

D
IS THE TRANSMISSION AN ACK MODE TRANSMISSION ?
2912
NO
YES
IS THERE AN ERROR IN THE RECEIVED PCPCH DATA PART?
2913
YES
2931
TRANSMIT NAK OVER FACH
2914
NO
TRANSMIT ACK OVER FACH
C
THE END OF CPCH RECEPTION PROCEDURE
2915

FIG. 29C